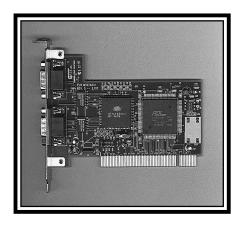
# JETPORT II

# Two Port PCI Serial Communcations Board



Installation Manual and User's Guide



Document number: 97-JP001 Ver 1.0 (9/10/97) dlh

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# **Chapter 1 - Introduction**

Thank you for purchasing the JetPort II. With the popularity of PCI based computers increasing, and in fact, becoming the standard, GTEK is pleased to offer the first *PCI Based* two port communications board. Previously, the performance and versatility of the 16C654 UART was limited to users requiring a large number of ports. But GTEK has brought this technology home to everyone.

Should you encounter a problem, our Technical Support staff are available to help you to achieve a successful installation, However, most problems can be resolved by careful reading of your User's Guide. Refer to **Chapter 4 - Troubleshooting**; before calling for technical support. Our business hours are 8:00 am to 5:00 pm Central Standard Time (CST) Monday through Friday, except holidays.

#### What's in this manual

This manual outlines the unpacking, installation, and use of the GTEK JetPort II PCI Serial Communications Board

# Included with the JetPort II PCI Communications Board

- · JetPort II PCI Serial Communications Board
- Cables; DE9 to DB25 (if ordered)
- Installation Manual and User's Guide
- Distribution diskette (see software license agreement)
- Warranty Card (please fill this out and return to GTEK)

## **Important static electricity precautions!**

Many computer components are sensitive to Electrostatic Discharge (ESD). The following steps reduce the possibility of damaging components with electrostatic discharge (static):

- Before handling any components or touching anything inside the computer, discharge your body's static electric charge by touching a grounded (earthed) surface. Wear a grounding wrist strap if one is available.
- Do not remove the board from its antistatic bag until you are ready to install it.
- Handle the board only by the edges and avoid touching the circuitry.
- Avoid sliding the board over any surface.
- Avoid having plastic, vinyl or foam in your work area.
- Limit your movements during installation; this reduces static electricity.

# **Warnings and Cautions**



It is very important that you disconnect the a.c. power cord to your computer before working inside your equipment.



It is always a good idea to back up your files before installing any new hardware!

# **Product Information Record**

Please record the important information below for handy reference. This will help us help you, in the event you need Technical Support.

Product Name:	JetPort II
Serial Number:	
Date Purchased:	
Purchased from:	

# **Chapter 2 - Hardware Setup**

# Before Installing the Interface board

The JetPort II is completely plug-and-play compatible. Generally all a user need do is install the board in the computer. WindowsNT 4.0 at this writing requires a simple installation program. In all cases, the computer's PCI bios makes all the decisions as to base address of each port and IRQ assignment. Should a problem be encountered in installation, refer to Section 4 for troubleshooting tips.

# Installing the Board

Follow these simple steps to install the JetPort II:

- Power down the system and remove the unit cover. Ground yourself by touching the metal chassis of the computer.
- 2. Locate a free PCI expansion slot.
- 3. Remove the screw securing the expansion port cover to the rear panel. *Don't lose the screw!*
- Seat the board firmly in the slot, taking care not to use excessive force.
- 5. Secure the card to the rear panel with the screw from step 3.
- 6. Replace the cover and power up the system.
- When connecting cables, the lower COM number is assigned to Port 1.

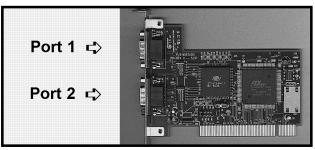


Figure 1 - Port Designation

# **Chapter 3 - Software Setup**

The distribution diskette shipped with your JetPort II contains the plug-and-play drivers for the JetPort II as well as the manual install program for WindowsNT. Follow the steps for your particular operating system.

#### Windows 95

Windows 95 has built-in plug-and-play which makes installing the JetPort II a snap. After installing the board, simply turn on the computer and allow Windows 95 to boot. During the course of initialization of the operating system, you will be presented with a screen indicating that a new PCI card has been detected (Figure 2).



Figure 2 - Windows 95 New Hardware Detect

Select "Driver from disk provided by hardware manufacturer" and click OK. Next you will be asked for a diskette (Figure 3). Be sure to enter which floppy drive the files are located on. Insert the distribution diskette in your floppy drive. Click OK.



Figure 3 - Install From Disk Dialog

At this point, the installation is totally automatic, with Windows 95 automatically assigning COM ports to the JetPort II. The COM port assignments may be viewed using Control Panel - System. Here the JetPort II is shown as a Multi-Function Adapter along with the two new ports, COM 5 and COM 6. Note that Windows 95 always starts non-bios ports at COM 5 and above.

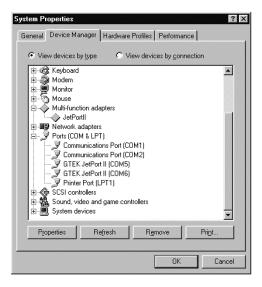


Figure 4 - Windows 95 System Properties

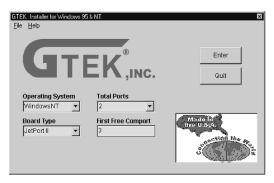


Figure 5 - Windows NT 4.0 Installer

#### WindowsNT 4.0

The GTEK Universal Installer for Windows 95/NT is used when installing the JetPort II under WindowsNT **ONLY**. Use the preceding procedure for Windows 95.

Carefully following the steps below will ensure a successful installation.

Insert the floppy. You may explore the floppy or use the Start Button and Run to execute the installer. The installation files are in a subdirectory called "WINNT", and the program you need to run is "SETUP.EXE". The files in the root directory of the floppy are for Windows 95 only.

Refer to Figure 5 and select using the pull-down menus the following parameters:

- Operating System (Here Windows NT).
- Select "Default" for the FIFO levels when the dialog box appears.
- Type of Board (JetPort II). Note that Base Address and IRQ boxes disappear as in the illustration. Your computer will determine these parameters automatically.
- First Port (if you are unsure, use the Control Panel,
   Ports applet to determine the next unused port)

 Total number of Ports (You may install one or both. It is suggested to install both even if you plan to use only one.)

If you desire to remove any ports associated with the JetPort II, use the CONTROL PANEL, PORTS applet to remove them.

# DOS, Windows 3.1, and Deskview

Support for these operating systems are provided through a utility placed in your autoexec.bat which will map the JetPort II in two of the standard DOS COM ports. They may be in the range of COM 1 to COM 4 depending upon the number of ports already installed in your computer. You must, however, make sure that there are two contiguous ports available. For example, if COM 1 and COM 2 already exist before running this utility, it will map the JetPort II in at COM 3 and COM 4.

Add the program "JETPORT.EXE" in the DOS subdirectory of your distribution disk to your **AUTOEXEC.BAT** file. You may type "JETPORT -h" at the command line for help.

# **Chapter 4 - Troubleshooting**

# **Technical Support**

GTEK provides one year of free technical support to our customers. Most problems can be diagnosed over the phone. If necessary, a replacement can be shipped out to you. Please have your GTEK Customer ID and invoice number ready when you call.

Our technicians greatest area of expertise is with the JetPort II itself. Although they may try to answer questions about peripherals and software setup, it is more efficient to contact the manufacturers directly. GTEK is not responsible for other vendors products.

# What to do before calling Tech Support

Please read through this troubleshooting section and review your install procedures. It is possible you may have configured the board improperly. Most technical support calls we handle are common problems that the user can remedy themselves. This section will help you determine if a technical support call is necessary.

- Check that all connections are secure and properly made.
- Check that all Jumpers are set correctly. Do not alter any jumper settings unless specifically instructed to do so by GTEK Technical Support.

#### **GTERM**

GTERM is a small utility program designed to help you determine if any ports are not working properly with the modems. This program is included on the distribution diskette.

# Using the GTERM program:

 Choose the Settings Menu and select the port you want to test. Connect a modem to that port.

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- Click Ok
- 3. Go to the Actions Menu and choose "Connect".
- A blinking cursor should appear in the window.
   Type the two letters "AT" and press ENTER. The modem should respond with "OK".
- 5. If an error message is returned, or if you cannot type "AT" at the prompt, check the installation settings, or verify that port is plugged into the right modem.

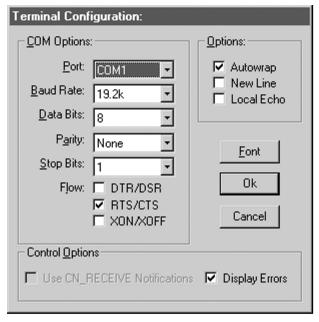


Figure 6 - GTERM Configuration Menu

# Getting Technical Support through the Internet

GTEK's Online Web and FTP sites are where you can download updated drivers and files, or send e-mail to our Technical Support Group. Our Web site is http://www.gtek.com and our FTP site is ftp.gtek.com. Technical support E-mail may be directed to spot@gtek.com.

# **Return Material Authorization (RMA)**

If we are unable to resolve your problem over the phone, and your product is still under warranty, we will gladly service your equipment at the factory. Refer to the limited warranty in this manual to learn about your specific rights and responsibilities.

You must call GTEK at (601)467-8048 and obtain an RMA number before you return any products to us. Put the RMA number on **EVERY** box you ship to us! Obtain an RMA number before you return equipment to avoid delays, accounting errors, or loss of the product.

- The technician who authorizes the return of your equipment will give you an RMA number. Write the number in LARGE, clear characters on the outside of each box you ship to us. Boxes received without an RMA number clearly visible will be refused by our receiving department.
- 2. Include a detailed description of the problem and also any conversations about problems you may have had with GTEK products. Include your Product Serial number, Invoice number and Product name. In case we have any questions, list the name and telephone number of the person directly responsible for maintaining the equipment.
- 3. Use the original box and packing material to protect the equipment from damage in shipment. Do not include unnecessary items such as software and manuals (unless we ask you to).

For your protection, insure the shipment for the full replacement value and use a reliable shipper. GTEK assumes no responsibility for equipment during shipment from customer to factory, whether in or out of warranty.

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The table below lists several common problems and their solutions. Double checking your setup will normally get things working.

Problem	Possible Solution
Operating system opens port, and modem TR light goes on, but port doesn't work.	Check to make sure that factory jumper settings have not been disturbed.
The operating system opens port, but TR light does not go on, no other problem evident.	Make sure modem is plugged in to correct channel.
Operating system says "error opening port" or "port not open".	Check to see that board shows up in Control Panel. Reinstallation might be necessary.
Port opens, can transmit/receive, but all that is transmitted /received is garbled.	Check the baud rate on your modem and/or the operating system settings for the port.
Port works, but phone won't answer, or distant modem answers, but fails to negotiate.	Check the init string and/or modem jumper settings.
Port opens, but can't transmit/receive.	Check the init string and/or modem jumper settings.

Table 4 - Solving Problems

# **Appendix -A Technical Specifications**

3.50" x 4.90"

Dimensions Bus Type Card Style I/O Addressing IRO 's Supported

PCL 32 Bit

Connectors

Automatically Assigned Automatically Assigned (PCI INT-A

through INT-D) DE-9

Data Cables

C2TM Telekit (DE-9 female to DB-25 male, six foot)

EIA-232 (RS-232C)

2

Interface Standard Number of I/O Ports Data Format Data Rates I/O Connector Config. Processor Type

UART FIFO Depth Handshake

Device Driver Support Environmental

Power Requirements

Modem Compatibility

Asynchronous, start + data + stop bits 110bps to 460.8Kbps (software selectable) DTE (Data Terminal Equipment) Intelligent UART 16C654 64 bytes transmit, 64 bytes receive

Driven by PC's processor or Auto-Handshake by UART WindowsNT, Windows95, DOS Operating Temperature: 0-70° degrees Celsius

Operating Humidity: 0-95% relative humidity (non-condensing) Powered by PCI bus: 5 VDC, 12 VDC, -12 VDC @ approximately 2 Watts Compatible with all serial interface modems including ISDN

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# Appendix - B

# **FCC Compliance Statement**

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesirable operation.

# **FCC Warning**

The user is cautioned that changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

# Appendix - C

#### **Warranty Information**

# **GTEK One-Year Limited Warranty**

GTEK, Inc. warrants to the original purchaser that this product, excluding items such as software, disks, and related documentation, will be free from defects in materials and/or workmanship for one (1) year from the date of purchase. During the warranty period, product determined by us to be defective in form or function will be repaired, or at our option, replaced at no charge. Shipping costs must be prepaid. Any replacements shall be new or serviceable used products, and are warranted for the remainder of the original warranty or thirty (30) days, whichever is longer. The warranty period is not extended as a result of purchasing any additional products from us or upgrading your JetPort II. The original purchaser must promptly notify GTEK in writing if there is a defect in material or workmanship. Written notice in all events must be received by GTEK before expiration of the warranty period. This warranty is not transferable.

#### International Warranty

The Warranty for international customers is the same as for customers within the United States, with the following exceptions: On all orders for replacement products, the customer must pay for the products and shipping costs before the products are shipped. When the defective products are returned to GTEK, GTEK will refund the cost of the products—shipping charges are not refundable. GTEK is not responsible for any custom fees, taxes or VAT that may be due. You must pay all custom fees, taxes or VAT that may be due.

This One-Year Limited Warranty covers normal use. GTEK does not warrant or cover:

- · damage during shipment other than original shipment to purchaser;
- damage caused by impact with other objects, dropping, falls, spilled liquids, or immersion in liquids;
- damage caused by disaster such as fire, flood, wind, earthquake, or lightning;
- damage caused by unauthorized attachments, alterations, modifications or foreign objects;
- damage caused by peripherals;
- defects caused by failure to provide a suitable installation environment for the product;
- damage caused by the use of the product for purposes other than those for which it was designed;
- damage from improper maintenance;
- · damage caused by any other abuse, misuse, mishandling, or misapplication.

Under no circumstances will GTEK, Inc. be liable for any special, incidental, or consequential damages based upon breach of warranty, breach of contract, negligence, strict liability, or any other legal theory. Such damages include but are not limited to, loss of profits, loss of revenue, loss of use of hardware system or

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any associated equipment, cost of capital, cost of substitute or replacement equipment, facilities or services, down time, purchaser's time, the claims of third parties, including customers, and injury to property.

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THIS DISCLAIMER OF WARRANTIES AND LIMITED WARRANTY ARE GOVERNED BY THE LAWS OF THE STATE OF MISSISSIPPI.

#### Replacement Products After the First Year

After the first year (which is defined as one year from the date of delivery of the GTEK product), the customer may purchase replacement products, if needed, from GTEK. The customer pays for labor to install replacement products, and shipping charges. This warranty applies only to products which were purchased from GTEK. The customer must provide the correct Customer ID. Under no circumstances will GTEK aid or assist in the unlicensed use of any type of software.

To obtain service under this warranty, please follow this procedure: With your customer ID and invoice # ready, call our technical service department: A technician will troubleshoot your problem over the phone. If the technician determines that a product is defective and that you should receive a replacement product, a replacement product will be sent to you at our expense. When you receive the replacement product, call our technical service department if you need assistance installing the product. A technician will walk you through the installation over the phone.

In the event we ask you to return the product for repair or replacement, please follow the instructions for Return Material Authorization (RMA). **DO NOT SEND EQUIPMENT TO GTEK WITHOUT AN RMA** #.

#### GTEK 30-Day Money Back Guarantee

GTEK is so confident in the quality of our products that we offer the original purchaser a money-back guarantee subject to the following terms and conditions:

- With your customer ID and invoice numbers ready, call your GTEK representative. If we cannot rectify the problem to your satisfaction, we will issue an RMA number and authorize the return of the product.
- 2. Ship the product back to us, freight prepaid and insured. Please pack it carefully, using the original box and packing material. Include all accessories, disks, cables, and manuals supplied with the system. Write the RMA number in large, clear characters on the outside of each box you send to us. GTEK assumes no responsibility for

- products during shipment from the customer to the factory.
- The product(s) must be in as-new, undamaged condition to receive credit.
- 4. To receive a refund, the product must be received at our factory within 30 days from the date on your invoice.
- Refunds for products purchased with a credit card will be paid by issuing a credit on your card. Shipping charges are not refundable.

#### Software License Agreement

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- 3) sublicense, rent, lease, or assign the Program.

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# Appendix - D

# UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

The following information is provided primarily for programmers desiring to write applications for the JetPort II.

#### **DESCRIPTION OF NEW FEATURES**

The 16C654 is designed to upgrade the existing 16C550 markets. It provides additional features to reduce the software over-head, external glue logic, operating stand-by current, and maintain the 16C550 software compatibility with existing software.

After reset, 16C654 is downward compatible with 16C454 / 68C454 and 16C554 / 68C554 except it provides 64 bytes of data FIFO (when 16C550 mode is enabled) instead of 16 bytes. All other additional features are available through special function register. The 16C654 offers the software/hardware flow control, sleep mode, selectable transmit trigger levels, and two selectable baud rate generators.

A separate FIFO ready register is provided to monitor the TXRDY and RXRDY of each individual UART to reduce polling time.

16C654 offers clock select pin for system / board designers to preset the baud rate table after reset. The CLKSEL pin selects the 1X or 1X/4 clock or internal baud rate generator. When CLKSEL is connected to the VCC pin the 1X clock is selected. 1X/4 clock is selected when CLKSEL is connected to GND.

#### **FUNCTIONAL DESCRIPTIONS**

The 64 byte data FIFO's are enabled when user writes to the 16C550 / 16C554 FIFO control register. With standard 16C550 parts, the user can only set receive trigger levels but not transmit trigger levels. The 16C654 provides independent trigger levels for both receiver and transmitter. To be compatible with 16C550, 1 byte transmit trigger level is selected after reset. The 16C654 is designed to work with high speed modems and shared network environments that require fast processing time. By increasing the number of characters in the FIFO, networking units can handle more data within the same time. Example: 16C550 with 16 bytes of data, 115.2Kbps and 8 bits wide word and 1 stop bit, will take 1.52 ms to transmit 16 bytes of data. But with 64 bytes of data buffer it will take 6.1 ms. This will give additional time for the CPU to process other applications and reduce the interrupt servicing time.

The contents of the Xon-1, 2 and Xoff 1, 2 are reset to "0" and user can write any values desired for software flow controls. Different conditions can be set to detect Xon/Xoff characters or start/stop the transmissions. See the table for all possible conditions. When single Xon/Xoff characters are selected, 16C654 compares the incoming data with these values and controls transmission, these characters are not stacked in data buffer or FIFO. When any Xon (MCR bit-5) bit is set, the 16C654 will resume the operation after receiving any character after recognizing the Xoff character. Note that the 16C654 will transmit Xon character(s) automatically when Xoff character(s) were sent and software flow control function were disabled afterwards. Special cases are provided to detect the special character and stack it into the data buffer or FIFO. These conditions are selected via Enhanced Feature Register (EFR bit 0-3).

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Hardware flow control can be selected when either or both bits of the EFR bit 6-7 are set to "1". When auto CTS is selected, the 16C654 will stop the transmission as soon as a complete character is transmitted and CTS input level is high. Transmission is resumed after CTS input changes to low level.

When auto RTS is selected, output of RTS pin is "AND-ed" with MCR bit-1 for manual over ride capability. RTS pin will change state when MCR bit-1 is set to "1". RTS pin will be forced to high state when receive FIFO reaches to the programmed trigger level. RTS pin resumes its original state after content of the data buffer (FIFO) drops below the next lower trigger level. Both hardware and software flow controls can be enabled for automatic operation. During these conditions the 16C654 will accept additional data to fill the unused transmit and receive FIFO locations.

Special interrupt modes have been added to monitor the hardware and software flow conditions. These are IER bits 5-7.

The 16C654 is designed to operate with low power consumption, special sleep mode has been added to stop the clock and reduce the power consumption when it is not used (Green PC). When EFR bit-4 and IER bit-4 are enabled (set to "1"), the 16C654 enters into sleep mode and resumes it's normal operation when data is received or state of the modem input pins changes or it is set to transmit data. The 16C654 stays in this mode until it is disabled

Special care should be considered for the following interrupt conditions and handling them. After reset, if the transmitter interrupt is enabled, 16C654 will issue an interrupt to indicate that transmit holding register is empty, no other interrupts will be issued after enabling the interrupt. The LSR register has highest interrupt priority and CTS, RTS have lowest priority. The interrupt status register will show the highest interrupt priority condition, and after servicing the interrupt condition, the next priority interrupt level will be shown. There are two interrupt conditions that have the same priority and it is important to know the conditions to service. Receive data ready and receive time out share the same priority with one additional bit (IER bit-3). Receiver issues interrupt after number of characters have reached the programmed trigger level. In this case the 16C654 FIFO holds equal or more characters than the trigger level. After reading a block of data, user can check the LSR bit-0 for additional characters.

Note that receive time out is functional only in 16C550/650 mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits) =  $4 \times P$  (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example-A: If user programs the word length = 7, and no parity and one stop bit, Time out will be: T = 4x7 (programmed word length) + 12 = 40 bits; Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example-B: If user programs the word length = 7, with parity and one stop bit, Time out will be: T = 4x7 (programmed word length) + 12 = 40 bits; Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1)] = 4 characters.

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Dual baud rate generator is provided to maintain the 16C550 compatibility and provide higher data rate when it is needed. Example: 14.4 Kbps to 19.2 Kbps modems required to have 57 Kbps to 115.2 Kbps data rate and 28.8 Kbps modems required to have 230.4 Kbps. The 16C550 compatible parts can only offer 115.2 Kbps to maintain the software compatibility. The 16C654 utilizes 7.32 MHz crystal/clock and provide 16C550 compatible data rate and higher. The 16C550 and 16C654 baud rate generator tables can be selected is setting and resetting the MCR bit-7. After hardware reset the 16C654 will set the baud rate table according to pin state of the CLKSEL.

The 16C654 transmit trigger level provides additional flexibility to the user for block mode operation. In 16C550/650 mode, LSR bits 5-6 gives indication that transmitter is empty or not, but there is no mechanism to identify FIFO full state or available empty locations in FIFO. User can select one of the two possible ways to operate the transmit and receive FIFO by utilizing the DMA mode (FCR bit-3). When FIFO's are enabled and DMA mode "0" is selected, the 16C654 sets the interrupt bit and activates interrupt output pin for single transmit and receive operation like 16C450 mode except that it can receive and transmit 64 bytes of characters. When DMA mode "1" is activated, user takes the advantage of the block mode operation. In this mode, the transmitter/receiver sets the interrupt flag and interrupt output pin, when characters in the FIFO are below the transmit trigger level or are over the receive trigger level. Note that since 16C550 does not have transmit trigger levels, the default trigger level in the 16C654 is set to 1 byte (trigger level "0").

#### SERIAL PORT SELECTION GUIDE

CS	A4	A3	UART X
1	X	X	X
0	0	0	UART A
0	0	1	UART B
0	1	0	UART C
0	1	1	UART D

This table is valid when 16/68 pin is connected to GND. Otherwise each UART is selected with individual CSx pins.

## **PROGRAMMING TABLE**

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	FIFO Control Register	
1	0	0	Line Control Register	
1	0	1	Line Status Register	Modem Control Register
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch
0	1	0	Enhanced Feature Register	Enhanced Feature Register
1	0	0	Xon-1 Word	Xon-1 Word
1	0	1	Xon-2 Word	Xon-2 Word
1	1	0	Xoff-1 Word	Xoff-1 Word
1	1	1	Xoff-2 Word	Xoff-2 Word

These registers are accessible only when LCR bit-7 is set to "1". Enhanced Feature Register, Xon1, 2 and Xoff1, 2 are accessible only when LCR is set to "BF".

## **REGISTER FUNCTIONAL DESCRIPTIONS**

#### TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the THR whenever the THR or TSR is empty. The THR empty flag will be set to "1" when the transmitter is empty or data is transferred to the TSR. Note that a write operation should be performed when the THR empty flag is set.

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On the falling edge of the start bit, the receiver internal counter will start to count 7 ½ clocks (16x clock) which is the center of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the LSR.

#### FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

- A. The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
- B. The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt is cleared when the FIFO drops below the trigger level.
- C. The data ready bit (LSR BIT-9) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

#### FIFO POLLED MODE OPERATION

When FCR BIT-0=1 the 16C654 is then in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the LSR.

- A. LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
- B. LSR BIT4-1 will specify which error(s) has occurred.
- LSR BIT-5 will indicate when the transmit FIFO is empty.
- D. LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
- E. LSR BIT-7 will indicate when there are any errors in the receive FIFO.

#### PROGRAMMABLE BAUD RATE GENERATOR

The 16C654 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 216 -1. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

# BAUD RATE GENERATOR PROGRAMMING TABLE (7.372 MHz CLOCK):

BAUD RATE MCR BIT-7=1	BAUD RATE MCR BIT-7=0	16 x CLOCK DIVISOR "Decimal"
50	200	2304
75	300	1536
150	600	768
300	1200	384
600	2400	192
1200	4800	96
2400	9600	48
4800	19.2Kbps	24
7200	28.8Kbps	16
9600	38.4Kbps	12
19.2Kbps	76.8Kbps	6
38.4Kbps	153.6Kbps	3
57.6Kbps	230.4Kbps	2
115.2Kbps	460.8Kbps	1

#### HARDWARE FLOW CONTROL OPERATION

When hardware flow control operation is enabled, the 16C654 monitors the CTS pin for transmit operation and receiver trigger level for RTS operation. When CTS changes state from low to high, the 16C654 suspends the transmission operation as soon as complete character is transmitted. ISR bit-5 will be set (if enabled via IER bit 6-7). Transmission will resume as soon as the CTS pin goes low. The RTS pin will be forced to a high state when the receiver FIFO reaches the programmed trigger level. RTS will go low when Receive Holding Register is below next lower trigger level. The 16C654 will accept additional data when transmission is suspended during hardware flow control till all locations are filled

Auto RTS is functional only when the MCR bit-1 is set to "1". The RST output pin can change state by setting MCR bit-1 to "0" or "1". This provides additional flexibility for manual over ride and maintains the hardware flow control functionality.

#### SOFTWARE FLOW CONTROL

When software flow control operation is enabled, the 16C654 will compare the two sequential receive data with Xoff-1, 2 programmed characters. When these characters are matched correctly, the 16C654 will halt the transmission after finishing the transmission of the complete character. The receive ready Xoff (if enabled via IER bit-5) flags will be set and the interrupt output pin (if receive interrupt is enabled) will be activated. After recognition of the Xoff characters the 16C654 will compare the next two incoming characters with Xon-1, 2 characters. The 16C654 will resume the operation and clear the flags (ISR bit-4) when Xon characters are received. The 16C654 will send Xoff-1, 2 characters as soon as received data reaches the programmed trigger level. The 16C654 will transmit programmed Xon-1, 2 characters as soon as receive data reaches the next lower trigger level.

# **INTERRUPT ENABLE REGISTER (IER)**

The Interrupt Enable Register (IER) masks incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

#### IER BIT-0:

0=disable the receiver ready interrupt 1=enable the receiver ready interrupt

#### IER BIT-1:

0=disable the transmitter empty interrupt 1=enable the transmitter empty interrupt

#### IER BIT-2:

0=disable the receiver line status interrupt 1=enable the receiver line status interrupt

#### IER BIT-3:

0=disable the modem status register interrupt 1=enable the modem status register interrupt

#### IER BIT-4:

0=disable sleep mode 1=enable sleep mode

(The 16C654 enters into power down mode and external clock or oscillator circuit is disabled. Any change of state on the RX, RI, CTS, DSR or CD pins start the 16C654. The 16C654 will not lose the programmed bits when sleep mode is activated or deactivated. The 16C654 will not enter sleep mode if any interrupt is pending.)

#### IER BIT-5:

0=disable received Xoff interrupt 1=enable received Xoff interrupt (The 16C654 issues an interrupt when Xoff characters are received and correctly match with Xoff 1, 2 words.)

#### IER BIT-6:

0=disable RTS interrupt

1=enable RTS interrupt (The 16C654 issues interrupt when RTS pin changes state from low to high.)

#### IER BIT-7:

0=disable CTS interrupt 1=enable CTS interrupt (The 16C654 issues interrupt when CTS pin changes state from low to high.)

# **INTERRUPT STATUS REGISTER (ISR)**

The 16C654 provides six level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the 16C654 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

#### ISR BIT-0:

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

1=no interrupt pending

#### **ISR BIT-1-3**:

Logical combination of these bits, provides the highest priority interrupt pending

#### **ISR BIT 4-5:**

These bits are enabled when EFR bit-4 is set to "1" ISR bit-4 indicates that matching Xoff characters have been detected. ISR bit-5 indicates that the CTS, RTS have been received or issued. Note that the ISR bit-4 will stay "1" until Xon characters are received.

#### **ISR BIT 6-7:**

These bits are not used and are set to "0" in 16C550 mode. BIT 6-7: are set to "1" in 16C654 mode

#### PRIORITY LEVEL

Р	D5	D4	D3	D2	D1	D0	Source of the Interrupt
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY (Received Data Ready)
2	0	0	1	1	0	0	RXRDY (Received Data time out)
3	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	0	0	MSR (Modem Status Register)
5	0	1	0	0	0	0	RXRDY (Received Xoff signal)/Special character
6	1	0	0	0	0	0	CTS, RTS change of state

#### **FIFO CONTROL REGISTER**

This register is used to enable the FIFO's, clear the FIFO's, set the receiver FIFO trigger level, and select the type of DMA signaling.

#### FCR BIT-0:

0=disable the transmit and receive FIFO 1=enable the transmit and receive FIFO This bit should be enabled before setting the FIFO trigger levels.

#### FCR BIT-1:

0=No change

1=clears the contents of the receive FIFO and resets the counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to "0" after clearing the FIFO's.

#### FCR BIT-2:

0=No change

1=clears the contents of the transmit FIFO and resets the counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to "0" after clearing the FIFO's.

#### FCR BIT-3:

0=No change

1=Changes RXRDY and TXRDY pins from mode "0" to mode "1"

### Transmit operation in mode "0":

When 16C654 is in 16C550 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY pin will go low. Once active, the TXRDY pin will go high (inactive) after the first character is loaded into the transmit holding register.

# Receive operation in mode "0":

When 16C654 is in 16C550 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY pin will go low. Once active, the RXRDY pin will go high (inactive) when there are no more characters in the receiver.

# Transmit operation in mode "1":

When 16C654 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) the TXRDY pin will go high (inactive) when the transmit FIFO is completely full. It will go low if one or more FIFO locations are empty.

# Receive operation in mode "1":

When 16C654 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) and the trigger level has been reached, the RXRDY pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

#### **FCR BIT 4-5:**

These bits are used to set the trigger level for the transmit FIFO interrupt. The 16C654 will issue a transmit empty interrupt when number of characters in FIFO drops below the selected trigger level.

BIT-5	BIT-4	FIFO Trigger Level
0	0	8
0	1	16
1	0	32
1	1	56

#### **FCR BIT 6-7:**

These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO Trigger Level
0	0	8
0	1	16
1	0	56
1	1	60

#### LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

#### LCR Bit 1-0:

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
		5.44

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1	0	7
1	1	8

#### LCR BIT-2:

The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5, 6, 7, 8	1
1	5	$1^{-1/2}$
1	6, 7, 8	2

#### LCR BIT-3:

Parity or no parity can be selected via this bit.

0=no parity

1= a parity bit is generated during the transmission, receiver also checks for received parity.

#### LCR BIT-4:

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=ODD parity is generated by forcing an odd number of 1's in the transmitted data. Receiver also checks for same format.

1=EVEN parity bit is generated by forcing an even number of 1's in the transmitted data. Receiver also checks for same format.

#### LCR BIT-5:

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

#### LCR Bit-6:

Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).

0=normal operating condition

1=forces the transmitter output (TX) to go low to alert the

communication terminal.

#### LCR BIT-7:

The internal baud rate counter latch and Enhanced Feature mode enable (DLAB).

0=normal operation

1=Divisor latch and Enhanced Feature register enable.

#### MODEM CONTROL REGISTER (MCR)

This register controls the interface between the MODEM or a peripheral device (RS232).

#### MCR BIT-0:

0=force DTR output to high 1=force DTR output to low

#### MCR BIT-1:

0=force RTS output to high 1=force RTS output to low

RTS is used as hardware flow control signal when enabled via EFR bit-6. RTS goes high when FIFO is reached to the selected trigger level and goes low as soon as content of the receive holding register is below the trigger level. Content of this register changes with state of the hardware flow control. Functions normally when hardware flow control is disabled.

#### MCR BIT-2:

This bit is used in internal loop-back mode only. 0=set OP1 output to high 1=set OP1 output to low

#### MCR BIT-3:

0=set OP2 output to high (internal loopback mode). Forces INTx outputs to three state mode if INTSEL pin is left open or connected to GND. It has no affect if INTSEL pin is connected to VCC.

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1=set OP2 output to low (internal loopback mode). Sets the INTx outputs to active mode if INTSEL pin is left open or connected to GND. It has no affect if INTSEL pin is connected to VCC.

#### MCR BIT-4:

0=normal operating mode

1=enable local loopback mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), STS, DSR, CD and RI are disabled. Internally the transmitter output is connected to the receiver input and DTR, RTS, OP1 and OP2 are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

#### MCR BIT-5:

0= disable Xon and function, 16C550 compatible 1=enable Xon any function

#### MCR BIT-6:

0=standard UART receive and transmit input/output 1=infrared receive and transmit input/output. The TX A-D outputs and RX A-D inputs are converted to infrared encoder/decoder output/input format. TX output goes low when this bit is set to "1".

#### MCR BIT-7:

0=normal or divide by one clock input. Standard 16C550 baud rates can be selected when this bit is set to "0" and 1.8432 MHz crystal is used.

1=divide by four clock input. Standard 16C550 baud rates can be selected when this bit is set to "1" and 7.372 crystal is used.

#### LINE STATUS REGISTER

This register provides the status of data transfer to CPU

#### LSR BIT-0:

0=no data in receive holding register or FIFO

1=data has been received and saved in the receive holding register or FIFO

#### LSR BIT-1:

0=no overrun error (normal)

1=overrun error, next character arrived before receive holding register was emptied or if FIFO's are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

#### LSR BIT-2:

0=no parity error (normal)

1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

#### LSR BIT-3:

0=no framing error (normal)

1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

#### LSR BIT-4:

0=no break condition (normal)

1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

#### LSR RIT-5:

It indicates that the 16C654 is ready to accept a new character for transmission. In addition, it causes the 16C654 to issue and interrupt to the CPU when the transmit holding register empty interrupt enable is set.

0=transmit holding register is not empty

1=transmit holding register (or FIFO) is empty. CPU can load the next characters. When this bit is set, CPU can load up to 64 bytes of data to the 16C654.

#### LSR BIT-6:

0=transmitter holding and shift registers are full 1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to "1" whenever the transmitter FIFO and transmit shift register are empty.

#### LSR BIT-7:

0=normal

1=at least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

#### MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

#### MSR BIT-0:

Indicates that the CTS input to the 16C654 has changed state since the last time it was read.

#### MSR BIT-1:

Indicates that the DSR input to the 16C654 has changed since the last time it was read.

#### MSR BIT-2:

Indicates that the RI input to the 16C654 has changed from a low to a high state.

#### MSR BIT-3:

Indicates that the CD input to the 16C654 has changed state since the last time it was read.

#### MSR BIT-4:

This bit is equivalent to RTS in the MCR during local loopback mode. It is the compliment of the CTS input.

CTS functions as hardware flow control signal input if it is enabled via EFR bit-7. Transmit holding register is gated with this input to start/stop the transmission. A high at this pin will stop the transmission as soon as complete character is transmitted.

#### MSR BIT-5:

This bit is equivalent to DTR in the MCR during local loopback mode. It is the compliment of the DSR input.

#### MSR BIT-6:

This bit is equivalent to OP1 in the MCR during local loopback mode. It is the compliment of the RI input.

#### MSR BIT-7:

This bit is equivalent to OP2 in the MCR during local loopback mode. It is the compliment of the CD input.

Note: whenever MSR bit 3-0 is set to logic "1", a MODEM Status Interrupt is generated.

# SCRATCHPAD REGISTER (SR)

16C654 provides a temporary data register to store 8 bits of information for variable use.

# **ENHANCED FEATURE REGISTER (EFR)**

Enhanced Feature Register can be enabled/disabled via this register.

#### EFR BIT 0-3:

Combinations of software flow control can be selected by programming these bits.

#### EFR BIT-4:

Enhanced functions enable bit

0=disables the IER bits 4-5, FCR bits 4-5 and MCR bits 5-7. After hardware reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are set to "0" to be compatible with 16C550 mode.

1=enables the enhanced functions. When this bit is set to "1" all enhanced features of the 16C654 are enabled. The content of IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 can be modified and latched. After modifying the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7, the EFR bit-4 can be set to "0" to latch the contents of the new values, this feature is provided to prevent the existing software's to alter/overwrite the 16C654 enhanced functions.

#### HANDSHAKE CONTROL BITS

Cont-Cont-Cont-Cont-		nt-Cont-	Tx, Rx software flow controls	
3	2	1	0	
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1 and Xon2 : Xoff1,
				Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1
X	X	0	1	Receiver compares Xon2, Xoff2
1	0	1	1	Transmit Xon1, Xoff1 Receiver
				compares Xon1, or Xon2 Xoff1 or
				Xoff2
0	1	1	1	Transmit Xon2, Xoff2 Receiver
				compares Xon1, or Xon2 Xoff1 or
				Xoff2
1	1	1	1	Transmit Xon1 and Xon2 : Xoff1,
				Xoff2 Receiver compares Xon1 and
				Xon2: Xoff1, Xoff2
0	0	1	1	No transmit flow control Receiver

compares Xon1 and Xon2 : Xoff1, Xoff?

#### EFR BIT-5

0=normal

1=special character detect

16C654 compares the incoming receive data with Xoff-2 data. Upon correct match, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character

#### EFR BIT-6:

RTS flow control

0=normal. RTS flow control is disabled. Standard 16C550 mode.

1=RTS pin goes high when receive FIFO's reach the programmed trigger level.

#### EFR BIT-7:

CTS flow control

0= normal. CTS flow control mode is disabled. Standard 16C550 mode.

1=transmission is resumed when low input signal is detected on the CTS pin.

#### FIFO READY REGISTER

This register provides the state of the transmit and receive FIFO.

# FIFORdy BIT 0-3:

0=transmit FIFO is full. The 16C654 can not take any more transmit data.

1=one or more empty locations in FIFO is below transmit trigger level.

# FIFORdy BIT 4-7:

0=receiver is above the trigger level or time-out has occurred. 1=receiver is not ready

#### 16C654 EXTERNAL RESET CONDITION

**REGISTERS**IER
RESET STATE
IER BITS 0-7=0

ISR EFR BIT-0=1, ISR BITS 1-7=0

LCR LCR BITS 0-7=0 MCR MCR BITS 0-7=0

LSR BITS 0-4=0; LSR BITS 5-6=1; LSR

BIT-7=0

MSR MSR BITS 0-3=0:

MSR BITS 4-7=INPUT SIGNALS

FCR FCR BITS 0-7=0 EFR EFR BITS 0-7=0

#### SIGNALS RESET STATE

TX A-D High
RTS A-D High
DTR A-D High
RXRDY A-D High
TXRDY A-D Low

# **CONNECTOR PINOUT**

# **DE-9 MALE (Board Connector)**

PIN	I/O	DESCRIPTION
1	<	DCD (Data Carrier Detect)
2	<	RX (Receive Data)
3	>	TX (Transmit Data)
4	>	DTR (Data Terminal Ready)
5		GND
6	<	DSR (Data Set Ready)
7	>	RTS (Request to Send)
8	<	CTS (Clear to Send)
9	<	RI (Ring Indicator)

# **DB-25 MALE (Telekit Cable)**

PIN	I/O	DESCRIPTION
1		EG (Equipment Ground)
2		\ 1 1 /
2	>	TX (Transmit Data)
3	<	RX (Receive Data)
4	>	RTS (Request to Send)
5	<	CTS (Clear to Send)
6	<	DSR (Data Set Ready)
7		GND (Signal Ground)
8	<	DCD (Data Carrier Detect)
20	>	DTR (Data Terminal Ready)
22	<	RI (Ring Indicator)

<sup>&</sup>lt; = To JetPort II

<sup>&</sup>gt; = To Modem or other DCE equipment

Use this chart for user constructed cabling. This connects the JetPort II to a DCE device. If you are connecting to DTE equipment, then a null-modem adapter is necessary.

DE9	DB25	DESCRIPTION
1	8	DCD (Data Carrier Detect)
2	3	RX (Receive Data)
3	2	TX (Transmit Data)
4	20	DTR (Data Terminal Ready)
5	7	GND (Signal Ground)
6	6	DSR (Data Set Ready)
7	4	RTS (Request to Send)
8	5	CTS (Clear to Send)
9	22	RI (Ring Indicator)