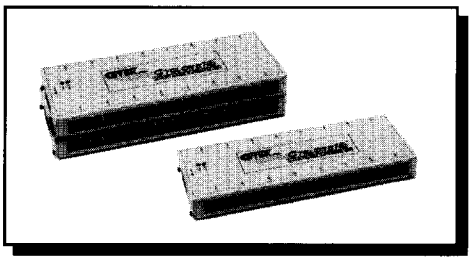
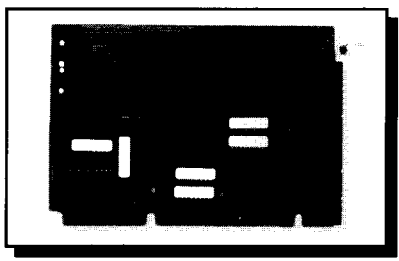
CYCLONE

Serial Expansion Units and Serial Boards





Installation Manual and User's Guide

GTEK®, INC.

Tomorrow's Communications Solutions

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Tables and Figures

Chapter 1 - Introduction

Thank you for purchasing the Cyclone Serial Expansion Unit. We feel this state-of-the-art technology will be the standard all other Intelligent Multiport serial communications boards will be measured against. Using the revolutionary 16C654 Intelligent UARTS, the Cyclone defines a new level of performance for intelligent serial communications.

Our Technical Support department is available to help you to achieve a successful installation. However, most answers can be found by careful reading of your User's Guide. Refer to **Chapter 4 - Troubleshooting**; before calling for technical support. Our business hours are 8:00 am to 5:00 pm Central Standard Time (CST) Monday through Friday, except holidays.

What's in this manual

The information provided in this manual is valid for the **Cyclone16 and Cyclone32 Serial Expansion Units**. If you purchased a **Cyclone 6**, there are special sections in Chapters 2 and 3 on this internal serial board. Most of the reference information is valid for all three products. Differences, where affected, are noted. Please take a few minutes to read this manual before installing your new Cyclone Serial Expansion Unit.

Cyclone Serial Expansion Unit

- ⇛ Cyclone16/32 Serial Expansion Unit (or Cyclone 6)
- ⇛ Interface (I/O) board (Cyclone16/32 ONLY)
- ⇛ Cables; DE9 to DB25 (if ordered)
- ⇛ Installation Manual and User's Guide
- ⇛ Distribution diskette (see software license agreement)
- ⇛ Warranty Card (please fill this out and return to GTEK)

Warnings and Cautions

Important static electricity precautions!

Many computer components are sensitive to Electrostatic Discharge (ESD). The following steps reduce the possibility of damaging components with electrostatic discharge (static):

- Before handling any components or touching anything inside the computer, discharge your body's static electric charge by touching a grounded (earthed) surface. Wear a grounding wrist strap if one is available.
- Do not remove the board from its antistatic bag until you are ready to install it.
- Handle the board only by the edges and avoid touching the circuitry.
- Avoid sliding the board over any surface.
- Avoid having plastic, vinyl or foam in your work area.
- Limit your movements during installation; this reduces static electricity.

WARNING!

It is very important that you disconnect the power supply to your system before installing expansion boards.

CAUTION!

Back up your system files before installing the I/O board or the software!

Product Information Record

Please record the important information below for handy reference. This will help us help you, in the event you need Technical Support.

Product Name: _____
Model Number: _____
Serial Number: _____
Date Purchased: _____
Purchased from: _____

Chapter 2 - Hardware Setup

Before Installing the Interface board

Before you install a new expansion board, you need to do a little research. **A little bit of time spent now, can save you a lot of troubleshooting later!** In order to set up the Cyclone properly, you'll need to determine two important system resources:

1. Available Interrupts (IRQ's)
2. Available I/O (Base) addresses

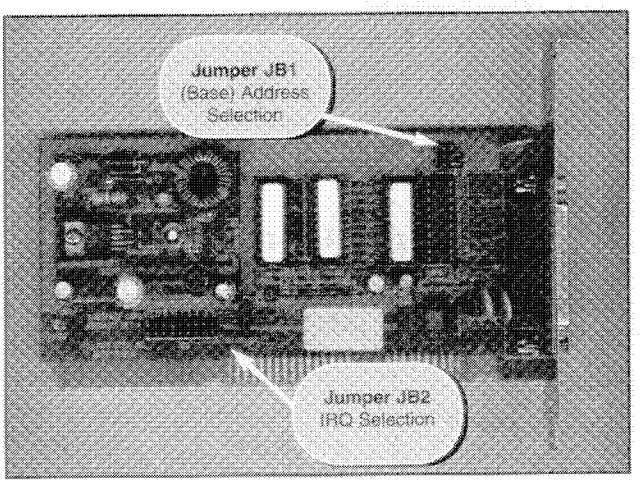

Figure 1 - Cyclone Interface Board (Cyclone16/32 ONLY)

Configuring Jumpers for IRQ and Base Address Selections

Many expansion boards have jumpers or switches which select interrupts and/or I/O addresses for the board. If these are not set correctly, the expansion board may conflict with another function in the computer. Please follow these instructions carefully to avoid these conflicts. *It will save you time and money!*

Note - See the Troubleshooting Guide for problems related to incorrectly setting the IRQ and Base Address.

A word about Interrupts

An interrupt suspends microprocessor program execution because a demand for attention from another peripheral device has been received. IRQ is an acronym for **I**nterrupt **ReQ**uest line.

IRQ	FUNCTION/ASSIGNMENT
NM I	Reports parity errors (Non-maskable Interrupt)
0	System Time
1	Keyboard
2	Cascades to IRQ9 (VGA or network cards)
3	COM 2
4	COM 1
5	LPT2 - parallel port 2
6	Disk Controller - hard and floppy disks
7	LPT1 - parallel port 2
8	Realtime clock interrupt
9	Software redirected to interrupt OA hex
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Primary hard disk controller
15	Secondary hard disk controller

Table 1 - Typical IRQ Assignments

Standard Interrupt Assignments

If a particular interrupt is not used in your system, you may assign it to something else. For example, if you don't have a second parallel port (LPT2) installed in your system, you can use IRQ 5 for another expansion card.

In some cases, you can share an interrupt between two devices that won't be used at the same time (a printer port and tape backup unit, for example). However, sharing interrupts between different devices can create a variety of problems, and should be avoided if at all possible.

If you install more than one Cyclone Serial Expansion Unit in one computer, each interface board must have its own interrupt.

Setting the IRQ Jumper:

1. Determine which free IRQ can be used (if required).
2. Locate JB2 on the I/O board (see the diagram below).
3. Move the jumper to the appropriate selection. Make sure it covers both pins.

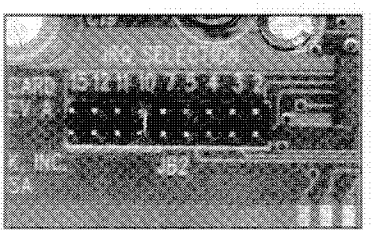

Figure 2 - IRQ Jumper (JB2) Cyclone16/32

Note: If you are installing the Cyclone 6, The IRQ Jumper is located at JB7. See the end of Chapter 2 for more information.

Deciding which I/O port addresses to use:

Each port on the Cyclone is controlled by a UART chip, occupying 8 contiguous bytes of I/O space. Therefore, since the Cyclone16 has 16 UARTS, it requires 128 bytes of contiguous I/O addressing space. For this reason, it is preferable to use one of the vertical addressing modes, (see Table 2) to avoid conflicts with other hardware devices. Port spacing for vertical addressing is 400h.

Example: The base address is set to 180h. In vertical mode addressing the next port would be addressed at 580h, 980h, 0d80h, and so on up to 4180h. The unit only occupies 10 bit PC I/O space of 180-187h and includes all the vertical aliases in this range.

Improper selection of an appropriate base address will not only cause some of the ports to not work properly, but may also cause conflicts with other devices.

When configuring 32 ports with the Cyclone32, a second group of 128 bytes of contiguous addressing space is 4000h above the first. If an address is taken up by another hardware device, you will have to choose another address range that can support the Cyclone. *Remember, you need 128 bytes of contiguous addressing space for the Cyclone16 and a second group of 128 bytes for the Cyclone32.* ***Refer to Appendix A-2 for more information.***

The Jumper blocks located on the I/O board (at JB1) need to be set for your particular base addressing situation. The table below is a guideline for selecting base addressing modes available for the Cyclone Serial Expansion Unit.

Pin 1	Pin 2	Pin 3	Addressing Mode	Notes
▮	▮	▮	0	vertical at 2f8 status 2ff COM2
▮	▮	▯	1	vertical at 3f8 status 3ff COM1
▮	▯	▮	2	vertical at 2e8 status 2ef COM4
▮	▯	▯	3	vertical at 3e8 status 3ef COM3
▯	▮	▮	4	vertical at 180 status 187
▯	▮	▯	5	vertical at 188 status 18f
▯	▯	▮	6	horizontal 100-17f status 200h
▯	▯	▯	7	horizontal 280-2ff status 201h

Table 2 - Addressing Modes for the Cyclone16/32

▮ Jumpered
▯ Not Jumpered

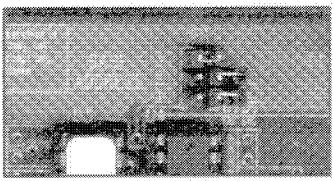

Figure 3 - Base Address Jumper (JB1)
Cyclone16/32

Note: Mode 7 may not be used with mode 0 or mode 2 simultaneously, since mode 7 contains COM2 and COM4. Modes 0-6 may be used simultaneously, providing up to 112 ports. Also, when using vertical addressing modes beginning with 3f8, 2f8, 3e8, 2e8, the operating system will see and install the first port as COM1, COM2, COM3 or COM4. Remember that there are only 15 more ports, and you may end up with the first port installed twice.

Important static electricity precautions!

Many computer components are sensitive to Electrostatic Discharge (ESD). The following steps reduce the possibility of damaging components with electrostatic discharge (static):

- Before handling any components or touching anything inside the computer, discharge your body's static electric charge by touching a grounded (earthed) surface. Wear a grounding wrist strap if one is available.
- Do not remove the board from its antistatic bag until you are ready to install it.
- Handle the board only by the edges and avoid touching the circuitry.
- Avoid sliding the board over any surface.
- Avoid having plastic, vinyl or foam in your work area.
- Limit your movements during installation; this reduces static electricity.

WARNING!

It is very important that you disconnect the power supply to your system before installing expansion boards.

CAUTION!

Back up your system files before installing the I/O board or the software!

Installing the Board

Choose your configuration options and set any jumpers on the interface board as necessary. (Refer to the previous section for important information on setting IRQ and I/O (Base) Address options)

1. Power down the system and remove the unit cover. Ground yourself by touching the metal chassis of the computer.
2. Locate a free expansion slot. Be sure to choose an appropriate slot for a 16-bit expansion card.
3. Remove the screw securing the expansion port cover to the rear panel. *Don't lose the screw!*
4. Seat the board firmly in the slot, taking care not to use excessive force.
5. Secure the card to the rear panel with the screw from step 4.
6. Connect one end of the DB-25 interface cable to the connector on the interface board. Connect the other end of the DB-25 connector to the Cyclone. Then, beginning with Port 1, connect the DE-9 to DB-25 cables to your modems.
7. Replace the cover and power up the system.

Cyclone 6 Setup

Thank you for purchasing GTEK's Cyclone 6. Below are a few guidelines that should make your installation go smoother. The installation manual you received was written for the Cyclone16/32, but most of the information related to installation is similar. A few important differences are noted here. It is highly recommended that you read through the installation manual before beginning the installation. It is also recommended that you back up your system files before proceeding with the installation.

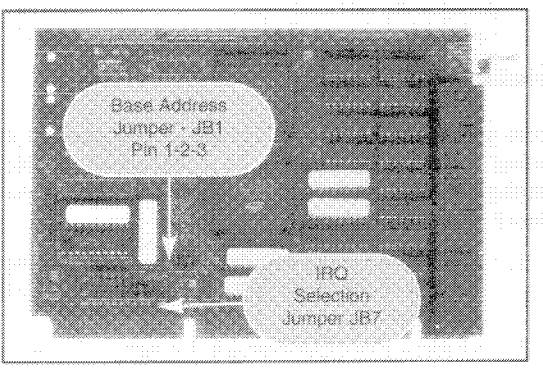

Figure 4 - Cyclone 6 Jumpers

Before Installing the Expansion board

Determine your system resources.

1. Available Interrupts (IRQ's) - Jumper JB7
2. Available I/O (Base) addresses - Jumper JB1

Please refer to pages 4 - 8 for general information on setting jumpers. Only Jumpers JB7 and JB1 need to be set. *Do not modify any other jumpers.*

Note: When using vertical addressing modes beginning with 3f8, 2f8, 3e8, 2e8, the operating system will see and install the first port as COM1, COM2, COM3 or COM4.

The Jumper blocks located on the I/O board (at JB1) need to be set for your particular base addressing situation. The pins are not numbered but are 1, 2, 3 from left to right. The table below is a guideline for selecting base addressing modes available for the Cyclone 6 ONLY.

Pin 1	Pin 2	Pin 3	Addressing Mode	Notes
▮	▮	▮	0	vertical at 2f8 status 2ff COM2
▮	▮	▯	1	vertical at 3f8 status 3ff COM1
▮	▯	▮	2	vertical at 2e8 status 2ef COM4
▮	▯	▯	3	vertical at 3e8 status 3ef COM3
▯	▮	▮	4	vertical at 180 status 187
▯	▮	▯	5	vertical at 188 status 18f
▯	▯	▮	6	horizontal 140-16f status 147h
▯	▯	▯	7	horizontal 280-2af status 287h

Table 3 - Addressing Modes for the Cyclone 6

▮ Jumpered
▯ Not Jumpered

Cables for the Cyclone 6 are RJ-45 to DB-25 type connectors with RS-232 interface. Optional RS-422 or RS-485 are also available.

Chapter 3 - Software Setup

Once you have installed the I/O board and connected all the required cables to the modems, you need to initialize the board. The distribution diskette shipped with your Cyclone Serial Expansion Unit contains install programs various operating systems. Follow the steps for your particular operating system below.

WindowsNT/Windows95

The GTEK Installer for Windows 95/NT is used when installing the Cyclone Serial Expansion Unit *or Cyclone 6* under WindowsNT or Windows 95. **See the "Readme First" Documentation for instructions on loading the install program.**

The steps below should ensure a successful installation. (Note: Steps 1-4 should have already been completed at this point)

Determine your system resources

1. Choose an available IRQ
2. Choose an available Base Address
3. Set the jumpers for these selections on the I/O board.
4. Remove power from your computer and install the interface board.
5. Boot to the operating system.

Make sure the selections you set on the interface board match the selection in the install program.

- Operating System
- Type of Board (Cyclone16, Cyclone32, Cyclone 6, etc.)
- I/O (Base) Address jumper setting
- IRQ jumper setting
- First Available Port (use the Control Panel)
- Total # of Ports

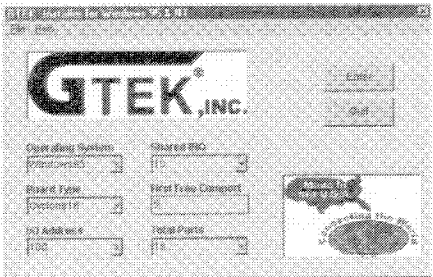

Figure - 5 GTEK's Install Program for WindowsNT/95

Once you have verified your choices, press ENTER. Exit all programs and reboot the operating system.

Important Note: If WindowsNT or Windows95 does not detect new hardware when you reboot, all is not lost! Recheck your configuration settings. This includes checking the I/O board for proper setup. There may be a conflict you missed. The program "GTERM" is included on the distribution diskette and can be used to test the ports after installation. See Chapter 4 - Troubleshooting for more information.

Linux

1. Run /linux/gtek install script provided on the distribution disk with the correct command line information:
   ;gtek 100 15 8 16
   (where 100 = base address, 15 = IRQ, 8 = offset, 16 (or 32) = number of ports.)
2. Type >cd/etc/rc.d
3. Type >rc.gtek
4. Reboot the Operating System
5. type: gtek —help for help.

DOS

Third party software or other user application is needed to setup the Cyclone Serial Expansion Board. Any type of FOSSIL driver can be used, such as XOO, which is available for download from our Customer Service BBS or FTP Site. Whatever the requirements, you will still need to set an IRQ and base address.

OS/2

Use of SIO by Ray Gwinn is required for installation. SIO can be downloaded from GTEK's BBS (and many others), or FTP Site. SIO can be used free and unregistered for the first four ports. See the license agreement for more information. Follow the programs documentation for setting up serial ports.

BSDI

Refer to file "GTEK" on your GTEK distribution diskette for a complete example config file. You should not need to specify an IRQ. BSDI should auto detect your configured IRQ on boot up. If you do need to select an IRQ, add 'irq ??' after the base I/O in your config file.

Software Setup for the Cyclone 6

Follow the same instructions for setting up the Cyclone16; choosing the appropriate parameters depending on your operating system.

Chapter 4 - Troubleshooting

Technical Support

GTEK provides one year of free technical support to our customers. Most problems can be diagnosed over the phone. If necessary, a replacement can be shipped out to you. Please have your GTEK Customer ID and invoice number ready when you call.

Our technicians greatest area of expertise is with the Cyclone Serial Expansion Unit itself. Although they may try to answer questions about peripherals and software setup, it is more efficient to contact the manufacturers directly. GTEK is not responsible for other vendors products.

What to do before calling Tech Support

Please read through this troubleshooting section and review your install procedures. It is possible you may have configured the board improperly. Most technical support calls we handle are common problems that the user can remedy themselves. This section will help you determine if a technical support call is necessary.

1. Check that all connections are secure and properly made.
2. Check that all Jumpers are set correctly. The only user configurable jumpers for the Cyclone16/32 are JB1 and JB2 (JB7 and JB1 for Cyclone 6). JB1 sets the base address and JB2 sets the IRQ. All other jumpers are factory set. Do not alter or remove these other jumper settings or the board may not work properly.
3. Make sure you have selected the correct IRQ and Base I/O Address jumper settings for your system. IRQ and base address selections need to be available (i.e., not in use or required by some other device), or else conflicts may occur.
4. Close all programs and reboot your computer after running the install program.

The table below lists several common problems and their solutions. Double checking your setup will normally get things working. Most problems are related to conflicts with the IRQ or I/O (Base) Address selection.

Problem	Possible Solution
Windows95 opens port, and TR light goes high, but port doesn't work.	Check that the IRQ setting (jumper and install program) is correct.
The operating system opens port, but TR light does not go high, no other problem evident.	Make sure modem is plugged in to correct channel.
Windows95/NT says "error opening port" or "port not open".	Check that the Base Address setting (board and install program) is correct.
Other devices that were working before, don't work now.	I/O address or IRQ conflicts with another device. Check your settings.
Port opens, can transmit/receive, but all that is transmitted /received is garbled.	Check the baud rate on your modem and/or the operating system settings for the port.
Port works, but phone won't answer, or distant modem answers, but fails to negotiate.	Check the init string and/or modem jumper settings.
Port opens, but can't transmit/receive.	Check the init string and/or modem jumper settings.
Ports work, but can't talk to port.	Verify IRQ settings.
Some ports work, some don't.	Check your modem, or swap with another working modem. IRQ is good, but Base Address on several channels conflict. Choose another Base Address.
When using IRQ 3 and 4, board doesn't work.	IRQ 3 & 4 are normally used by COM 1 & COM2. Choose another IRQ or, disable COM1 or COM2 (in system BIOS)

Table 4 - Solving Problems

GTERM

GTERM is a small utility program designed to help you determine if any ports are not working properly with the modems. The program is included on the distribution diskette.

Using the GTERM program:

1. Choose the Settings Menu and set up the port you want to test.
2. Press Ok.
3. Go to the Actions Menu and choose "Connect".
4. A blinking cursor should appear in the window. Type >AT and return. You should see a message that says the port is working properly.
5. If "Port Not Open" is returned, if you can not type "AT" at the prompt, check the program settings, or that the port is plugged into the right modem.

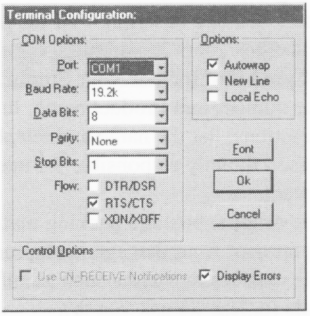

Figure 6 - GTERM Utility Program

Getting Technical Support through the BBS

GTEK's Customer Service BBS is where you can download drivers and files, or send e-mail to the technicians and ask questions. It is also used as a test bed for our products. *For this reason, dial-up capabilities may not always be available.* If you have a need to dial-in and it does not appear to be up, call (601) 467-8048 during normal business hours. You can Telnet to the BBS at bbs.gtek.com or dial in (601) 466-0506.

Return Material Authorization (RMA)

If we are unable to resolve your problem over the phone, and your product is still under warranty, we will gladly service your equipment at the factory. Refer to the limited warranty in this manual to learn about your specific rights and responsibilities.

You must call GTEK at (601)467-8048 and obtain an RMA number before you return any products to us. Put the RMA number on every box you ship to us! Obtain an RMA number before you return equipment to avoid delays, accounting errors, or loss of the product.

1. The technician who authorizes the return of your equipment will give you an RMA number. Write the number in large, clear characters on the outside of each box you ship to us. Boxes received without an RMA number clearly visible will be refused by our receiving department.
2. Include a detailed description of the problem and conversations about the problems you have had with GTEK products. Include your Product Serial number, Invoice number and Product name. In case we have any questions, list the name and telephone number of the person directly responsible for maintaining the equipment.
3. Use the original box and packing material to protect the equipment from damage in shipment. Do not include unnecessary items such as software and manuals (unless we ask you to).

For your protection, insure the shipment for the full replacement value and use a reliable shipper. GTEK assumes no responsibility for equipment during shipment from customer to factory, whether in or out of warranty.

APPENDICES

Appendix -A Technical Specifications

Dimensions	4.25" x 6.75"
Bus Type	ISA Card Slot
Card Style	16-bit fi -size
I/O Addressing	8 modes available; 2 horizontal and 6 vertical modes
IRQ 's Supported	9 selections available: 2,3,4,5,7,10,11,12,15
Connectors	RJ-45
Data Cables	Cyclone16: C16TM Telekit: 16-6 foot RJ-45 to DB-25M (optional), 1-6 foot interface cable (included) Cyclone 6: B6TM Telekit: 6-6 foot RJ-45 to DB-25M (optional)
Interface Standard	EIA-232 (RS-232C)
Optional Interface	RS-422 or RS-485
Number of I/O Ports	6, 16 or 32
Data Format	Asynchronous, start + data + stop bits
Data Rates	110bps to 460.8Kbps (software selectable)
I/O Connector Config.	DTE (Data Terminal Equipment)
Processor Type	Intelligent UART
UART	16C654
FIFO Depth	64 bytes transmit, 64 bytes receive
Handshake	Driven by PC's processor or Auto-Handshake by UART
Device Driver Support	WindowsNT, Windows95, FreeBSD, BSDI, Linux, DOS, OS/2 (SIO), XOO
Environmental	Operating Temperature: 0-70° degrees Celsius Operating Humidity: 0-95% relative humidity (non-condensing)
Power Requirements	Powered by ISA bus: 5 VDC, 12 VDC, -12 VDC @ 5 Watts
Modem Compatibility	Compatible with all RS-232 type modems including ISDN

Appendix A-3
Port Spacing for the Cyclone16/32 (refer to page 7 for status)

Port Spacing for the Cyclone 16

MODE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	2f8	6f8	af8	ef8	12f8	16f8	1af8	1ef8	22f8	26f8	2af8	2ef8	32f8	36f8	3af8	3ef8
1	3f8	7f8	bf8	ff8	13f8	17f8	1bf8	1ff8	23f8	27f8	2bf8	2ff8	33f8	37f8	3bf8	3ff8
2	2e8	6e8	ae8	ee8	12e8	16e8	1ae8	1ee8	22f8	26f8	2af8	2ef8	32f8	36f8	3af8	3ef8
3	3e8	7e8	be8	fe8	13e8	17e8	1be8	1fe8	23e8	27e8	2be8	2fe8	33e8	37e8	3be8	3fe8
4	180	580	980	d80	1180	1580	1980	1d80	2180	2580	2980	2d80	3180	3580	3980	3d80
5	188	588	988	d88	1188	1588	1988	1d88	2188	2588	2988	2d88	3188	3588	3988	3d88
6	100	108	110	118	120	128	130	138	140	148	150	158	160	168	170	178
7	280	288	290	298	2a0	2a8	2b0	2b8	2c0	2c8	2d0	2d8	2e0	2e8	2f0	2f8

Port Spacing for the Cyclone 32

MODE	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
0	42f8	46f8	4af8	4ef8	52f8	56f8	5af8	5ef8	62f8	66f8	6af8	6ef8	72f8	76f8	7af8	7ef8
1	43f8	47f8	4bf8	4ff8	53f8	57f8	5bf8	5ff8	63f8	67f8	6bf8	6ff8	73f8	77f8	7bf8	7ff8
2	42e8	46e8	4ae8	4ee8	52e8	56e8	5ae8	5ee8	62e8	66e8	6ae8	6ee8	72e8	76e8	7ae8	7ee8
3	43e8	47e8	4be8	4fe8	53e8	57e8	5be8	5fe8	63e8	67e8	6be8	6fe8	73e8	77e8	7be8	7fe8
4	4180	4580	4980	4d80	5180	5580	5980	5d80	6180	6580	6980	6d80	7180	7580	7980	7d80
5	4188	4588	4988	4d88	5188	5588	5988	5d88	6188	6588	6988	6d88	7188	7588	7988	7d88
6	4100	4108	4110	4118	4120	4128	4130	4138	4140	4148	4150	4158	4160	4168	4170	4178
7	4280	4288	4290	4298	42a0	42a8	42b0	42b8	42c0	42c8	42d0	42d8	42e0	42e8	42f0	42f8

Appendix A-3
Port Spacing for the Cyclone 6 (refer to page 11 for status)

Port Spacing for the Cyclone 6

MODE	1	2	3	4	5	6
0	2f8	6f8	af8	ef8	12f8	16f8
1	3f8	7f8	bf8	ff8	13f8	17f8
2	2e8	6e8	ae8	ee8	12e8	16e8
3	3e8	7e8	be8	fe8	13e8	17e8
4	180	580	980	d80	1180	1580
5	188	588	988	d88	1188	1588
6	140	148	150	158	160	168
7	280	288	290	298	2a0	2a8

Appendix - B

FCC Compliance Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesirable operation.

FCC Warning

The user is cautioned that changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

Appendix - C

Warranty Information

GTEK One-Year Limited Warranty

GTEK, Inc. warrants to the original purchaser that this product, excluding items such as software, disks, and related documentation, will be free from defects in materials and/or workmanship for one (1) year from the date of purchase. During the warranty period, product determined by us to be defective in form or function will be repaired, or at our option, replaced at no charge. Shipping costs must be prepaid. Any replacements shall be new or serviceable used products, and are warranted for the remainder of the original warranty or thirty (30) days, whichever is longer. The warranty period is not extended as a result of purchasing any additional products from us or upgrading your Cyclone Serial Expansion Unit. The original purchaser must promptly notify GTEK in writing if there is a defect in material or workmanship. Written notice in all events must be received by GTEK before expiration of the warranty period. This warranty is not transferable.

International Warranty
The Warranty for international customers is the same as for customers within the United States, with the following exceptions: On all orders for replacement products, the customer must pay for the products and shipping costs before the products are shipped. When the defective products are returned to GTEK, GTEK will refund the cost of the products—shipping charges are not refundable. GTEK is not responsible for any custom fees, taxes or VAT that may be due. You must pay all custom fees, taxes or VAT that may be due.

This One-Year Limited Warranty covers normal use. GTEK does not warrant or cover:

- damage during shipment other than original shipment to purchaser;
- damage caused by impact with other objects, dropping, falls, spilled liquids, or immersion in liquids;
- damage caused by disaster such as fire, flood, wind, earthquake, or lightning;
- damage caused by unauthorized attachments, alterations, modifications or foreign objects;
- damage caused by peripherals;
- defects caused by failure to provide a suitable installation environment for the product;
- damage caused by the use of the product for purposes other than those for which it was designed;
- damage from improper maintenance;
- damage caused by any other abuse, misuse, mishandling, or misapplication.

Under no circumstances will GTEK, Inc. be liable for any special, incidental, or consequential damages based upon breach of warranty, breach of contract, negligence, strict liability, or any other legal theory. Such damages include but are not limited to, loss of profits, loss of revenue, loss of use of hardware system or

any associated equipment, cost of capital, cost of substitute or replacement equipment, facilities or services, down time, purchaser's time, the claims of third parties, including customers, and injury to property.

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THIS DISCLAIMER OF WARRANTIES AND LIMITED WARRANTY ARE GOVERNED BY THE LAWS OF THE STATE OF MISSISSIPPI.

Replacement Products After the First Year
After the first year (which is defined as one year from the date of delivery of the GTEK product), the customer may purchase replacement products, if needed, from GTEK. The customer pays for labor to install replacement products, and shipping charges. This warranty applies only to products which were purchased from GTEK. The customer must provide the correct Customer ID. Under no circumstances will GTEK aid or assist in the unlicensed use of any type of software.

To obtain service under this warranty, please follow this procedure:
With your customer ID and invoice # ready, call our technical service department: A technician will troubleshoot your problem over the phone. If the technician determines that a product is defective and that you should receive a replacement product, a replacement product will be sent to you at our expense.
When you receive the replacement product, call our technical service department if you need assistance installing the product. A technician will walk you through the installation over the phone.
In the event we ask you to return the product for repair or replacement, please follow the instructions for Return Material Authorization (RMA). **DO NOT SEND EQUIPMENT TO GTEK WITHOUT AN RMA #.**

GTEK 30-Day Money Back Guarantee
GTEK is so confident in the quality of our products that we offer the original purchaser a money-back guarantee subject to the following terms and conditions:

1. With your customer ID and invoice numbers ready, call your GTEK representative. If we cannot rectify the problem to your satisfaction, we will issue an RMA number and authorize the return of the product.
2. Ship the product back to us, freight prepaid and insured. Please pack it carefully, using the original box and packing material. Include all accessories, disks, cables, and manuals supplied with the system. Write the RMA number in large, clear characters on the outside of each box you send to us. GTEK assumes no responsibility for

products during shipment from the customer to the factory.

3. The product(s) must be in as-new, undamaged condition to receive credit.
4. To receive a refund, the product must be received at our factory *within 30 days* from the date on your invoice.
5. Refunds for products purchased with a credit card will be paid by issuing a credit on your card. ***Shipping charges are not refundable.***

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Appendix - D

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

The following information is provided for your convenience

DESCRIPTION OF NEW FEATURES

The 16C654 is designed to upgrade the existing 16C550 market. It provides additional features to reduce the software over-head, external glue logic, operating stand-by current, and maintain the 16C550 software compatibility with existing software's.

After reset, 16C654 is downward compatible with 16C454 / 68C454 and 16C554 / 68C554 except it provides 64 bytes of data FIFO (when 16C550 mode is enabled) instead of 16 bytes. All other additional features are available through special function register. The 16C654 offers the software/hardware flow control, sleep mode, selectable transmit trigger levels, and two selectable baud rate generators.

A separate FIFO ready register is provided to monitor the TXRDY and RXRDY of each individual UART to reduce polling time.

16C654 offers clock select pin for system / board designers to preset the baud rate table after reset. The CLKSEL pin selects the 1X or 1X/4 clock or internal baud rate generator. When CLKSEL is connected to the VCC pin the 1X clock is selected. 1X/4 clock is selected when CLKSEL is connected to GND.

FUNCTIONAL DESCRIPTIONS

The 64 byte data FIFO's are enabled when user writes to the 16C550 / 16C554 FIFO control register. With standard 16C550 parts, the user can only set receive trigger levels but not transmit trigger levels. The 16C654 provides independent trigger levels for both receiver and transmitter. To be compatible with 16C550, 1 byte transmit trigger level is selected after reset. The 16C654 is designed to work with high speed modems and shared network environments that require fast processing time. By increasing the number of characters in the FIFO, networking units can handle more data within the same time. Example: 16C550 with 16 bytes of data, 115.2Kbps and 8 bits wide word and 1 stop bit, will take 1.52 ms to transmit 16 bytes of data. But with 64 bytes of data buffer it will take 6.1 ms. This will give additional time for the CPU to process other applications and reduce the interrupt servicing time.

The contents of the Xon-1, 2 and Xoff 1, 2 are reset to "0" and user can write any values desired for software flow controls. Different conditions can be set to detect Xon/Xoff characters or start/stop the transmissions. See the table for all possible conditions. When single Xon/Xoff characters are selected, 16C654 compares the incoming data with these values and controls transmission, these characters are not stacked in data buffer or FIFO. When any Xon (MCR bit-5) bit is set, the 16C654 will resume the operation after receiving any character after recognizing the Xoff character. Note that the 16C654 will transmit Xon character(s) automatically when Xoff character(s) were sent and software flow control function were disabled afterwards. Special cases are provided to detect the special character and stack it into the data buffer or FIFO. These conditions are selected via Enhanced Feature Register (EFR bit 0-3).

Hardware flow control can be selected when either or both bits of the EFR bit 6-7 are set to "1". When auto CTS is selected, the 16C654 will stop the transmission as soon as a complete character is transmitted and CTS input level is high. Transmission is resumed after CTS input changes to low level.

When auto RTS is selected, output of RTS pin is "AND-ed" with MCR bit-1 for manual over ride capability. RTS pin will change state when MCR bit-1 is set to "1". RTS pin will be forced to high state when receive FIFO reaches to the programmed trigger level. RTS pin resumes its original state after content of the data buffer (FIFO) drops below the next lower trigger level. Both hardware and software flow controls can be enabled for automatic operation. During these conditions the 16C654 will accept additional data to fill the unused transmit and receive FIFO locations.

Special interrupt modes have been added to monitor the hardware and software flow conditions. These are IER bits 5-7.

The 16C654 is designed to operate with low power consumption, special sleep mode has been added to stop the clock and reduce the power consumption when it is not used (Green PC). When EFR bit-4 and IER bit-4 are enabled (set to "1"), the 16C654 enters into sleep mode and resumes it's normal operation when data is received or state of the modem input pins changes or it is set to transmit data. The 16C654 stays in this mode until it is disabled.

Special care should be considered for the following interrupt conditions and handling them. After reset, if the transmitter interrupt is enabled, 16C654 will issue an interrupt to indicate that transmit holding register is empty, no other interrupts will be issued after enabling the interrupt. The LSR register has highest interrupt priority and CTS, RTS have lowest priority. The interrupt status register will show the highest interrupt priority condition, and after servicing the interrupt condition, the next priority interrupt level will be shown. There are two interrupt conditions that have the same priority and it is important to know the conditions to service. Receive data ready and receive time out share the same priority with one additional bit (IER bit-3). Receiver issues interrupt after number of characters are reached the programmed trigger level, in this case the 16C654 FIFO holds equal or more characters than the trigger level. After reading a block of data, user can check the LSR bit-0 for additional characters.

Note that receive time out is functional only in 16C550/650 mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits) = 4 x P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example-A: If user programs the word length = 7, and no parity and one stop bit, Time out will be: T= 4x7 (programmed word length) + 12 = 40 bits; Character time = 40 / 9 [(programmed word length = 7) + (stop bit =1) + (start bit = 1)] = 4.4 characters.

Example-B: If user programs the word length = 7, with parity and one stop bit, Time out will be: T= 4x7 (programmed word length) + 12 = 40 bits; Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit =1) + (start bit = 1)] = 4 characters.

Dual baud rate generator is provided to maintain the 16C550 compatibility and provide higher data rate when it is needed. Example: 14.4 Kbps to 19.2 Kbps modems required to have 57 Kbps to 115.2 Kbps data rate and 28.8 Kbps modems required to have 230.4 Kbps. The 16C550 compatible parts can only offer 115.2 Kbps to maintain the software compatibility. The 16C654 utilizes 7.32 MHz crystal/clock and provide 16C550 compatible data rate and higher. The 16C550 and 16C654 baud rate generator tables can be selected is setting and resetting the MCR bit-7. After hardware reset the 16C654 will set the baud rate table according to pin state of the CLKSEL.

The 16C654 transmit trigger level provides additional flexibility to the user for block mode operation. In 16C550/650 mode, LSR bits 5-6 gives indication that transmitter is empty or not, but there is no mechanism to identify FIFO full state or available empty locations in FIFO. User can select one of the two possible ways to operate the transmit and receive FIFO by utilizing the DMA mode (FCR bit-3). When FIFO's are enabled and DMA mode "0" is selected, the 16C654 sets the interrupt bit and activates interrupt output pin for single transmit and receive operation like 16C450 mode except it can receive and transmit 64 bytes of characters. When DMA mode "1" is activated, user takes the advantage of the block mode operation. In this mode, transmitter/receiver sets the interrupt flag and interrupt output pin, when characters in the FIFO are below the transmit trigger level or over receive trigger level. Note that since 16C550 does not have transmit trigger levels, the default trigger level in the 16C654 is set to 1 byte (trigger level "0").

SERIAL PORT SELECTION GUIDE

CS	A4	A3	UART X
1	x	x	x
0	0	0	UART A
0	0	1	UART B
0	1	0	UART C
0	1	1	UART D

This table is valid when 16/68 pin is connected to GND. Otherwise each UART is selected with individual CSx pins.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	FIFO Control Register	
1	0	0	Line Control Register	
1	0	1	Line Status Register	Modem Control Register
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch
0	1	0	Enhanced Feature Register	Enhanced Feature Register
1	0	0	Xon-1 Word	Xon-1 Word
1	0	1	Xon-2 Word	Xon-2 Word
1	1	0	Xoff-1 Word	Xoff-1 Word
1	1	1	Xoff-2 Word	Xoff-2 Word

These registers are accessible only when LCR bit-7 is set to "1". Enhanced Feature Register, Xon1, 2 and Xoff1, 2 are accessible only when LCR is set to "BF".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the THR whenever the THR or TSR is empty. The THR empty flag will be set to "1" when the transmitter is empty or data is transferred to the TSR. Note that a write operation should be performed when the THR empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 fi clocks (16x clock) which is the center of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the LSR.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A. The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
B. The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt is cleared when the FIFO drops below the trigger level.
C. The data ready bit (LSR BIT-9) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1 puts the 16C654 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the LSR.

A. LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
B. LSR BIT4-1 will specify which error(s) has occurred.
C. LSR BIT-5 will indicate when the transmit FIFO is empty.
D. LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
E. LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR

The 16C654 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 216 -1. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

BAUD RATE GENERATOR PROGRAMMING TABLE (7.372 MHz CLOCK):

BAUD RATE MCR BIT-7=1	BAUD RATE MCR BIT-7=0	16 x CLOCK DIVISOR "Decimal"
50	200	2304
75	300	1536
150	600	768
300	1200	384
600	2400	192
1200	4800	96
2400	9600	48
4800	19.2Kbps	24
7200	28.8Kbps	16
9600	38.4Kbps	12
19.2Kbps	76.8Kbps	6
38.4Kbps	153.6Kbps	3
57.6Kbps	230.4Kbps	2
115.2Kbps	460.8Kbps	1

HARDWARE FLOW CONTROL OPERATION

When hardware flow control operation is enabled, the 16C654 monitors the CTS pin for transmit operation and receiver trigger level for RTS operation. When CTS changes state from low to high, the 16C654 suspends the transmission operation as soon as complete character is transmitted. ISR bit-5 will be set (if enabled via IER bit 6-7). Transmission will resume as soon as CTS pin goes low. RTS pin will be forced to high state when receiver FIFO reached to the programmed trigger level. RTS will go low when Receive Holding Register is below next lower trigger level. The 16C654 will accept additional data when transmission is suspended during hardware flow control till all locations are filled.

Auto RTS is functional only when the MCR bit-1 is set to "1". The RST output pin can change state by setting MCR bit-1 to "0" or "1". This provides additional flexibility for manual over ride and maintain the hardware flow control functionality.

SOFTWARE FLOW CONTROL

When software flow control operation is enabled, the 16C654 will compare the two sequential receive data with Xoff-1, 2 programmed characters. When these characters are matched correctly, the 16C654 will halt the transmission after finishing the transmission of the complete character. The receive ready Xoff (if enabled via IER bit-5) flags will be set and the interrupt output pin (if receive interrupt is enabled) will be activated. After recognition of the Xoff characters the 16C654 will compare the next two incoming characters with Xon-1, 2 characters. The 16C654 will resume the operation and clear the flags (ISR bit-4) when Xon characters are received. The 16C654 will send Xoff-1, 2 characters as soon as received data passed the programmed trigger level. The 16C654 will transmit programmed Xon-1, 2 characters as soon as receive data reached to the next lower trigger level.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt
1=enable the receiver ready interrupt
IER BIT-1:
0=disable the transmitter empty interrupt
1=enable the transmitter empty interrupt
IER BIT-2:
0=disable the receiver line status interrupt
1=enable the receiver line status interrupt
IER BIT-3:
0=disable the modem status register interrupt
1=enable the modem status register interrupt
IER BIT-4:
0=disable sleep mode
1=enable sleep mode

(The 16C654 enters into power down mode and external clock or oscillator circuit is disabled. Any change of state on the RX, RI, CTS, DSR or CD pins start the 16C654. The 16C654 will not lose the programmed bits when sleep mode is activated or deactivated. The 16C654 will not enter sleep mode if any interrupt is pending.)

IER BIT-5:
0=disable received Xoff interrupt
1=enable received Xoff interrupt
(The 16C654 issues an interrupt when Xoff characters are received and correctly match with Xoff 1, 2 words.)

IER BIT-6:
0=disable RTS interrupt
1=enable RTS interrupt
(The 16C654 issues interrupt when RTS pin changes state from low to high.)

IER BIT-7:
0=disable CTS interrupt
1=enable CTS interrupt
(The 16C654 issues interrupt when CTS pin changes state from low to high.)

INTERRUPT STATUS REGISTER (ISR)

The 16C654 provides six level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the 16C654 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending

ISR BIT-1-3:
Logical combination of these bits, provides the highest priority interrupt pending

ISR BIT 4-5:
These bits are enabled when EFR bit-4 is set to "1" ISR bit-4 indicates that matching Xoff characters have been detected. ISR bit-5 indicates that the CTS, RTS have been received or issued . Note that the ISR bit-4 will stay "1" until Xon characters are received.

ISR BIT 6-7:
These bits are not used and are set to "0" in 16C550 mode. BIT 6-7: are set to "1" in 16C654 mode.

PRIORITY LEVEL

P	D5	D4	D3	D2	D1	D0	Source of the Interrupt
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY (Received Data Ready)
2	0	0	1	1	0	0	RXRDY (Received Data time out)
3	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	0	0	MSR (Modem Status Register)
5	0	1	0	0	0	0	RXRDY (Received Xoff signal)/Special character
6	1	0	0	0	0	0	CTS, RTS change of state

FIFO CONTROL REGISTER

This register is used to enable the FIFO's, clear the FIFO's, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=disable the transmit and receive FIFO
1=enable the transmit and receive FIFO
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change
1=clears the contents of the receive FIFO and resets the counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to "0" after clearing the FIFO's.

FCR BIT-2:

0=No change
1=clears the contents of the transmit FIFO and resets the counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to "0" after clearing the FIFO's.

FCR BIT-3:

0=No change
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1"

Transmit operation in mode "0":

When 16C654 is in 16C550 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY pin will go low. Once active, the TXRDY pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":

When 16C654 is in 16C550 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY pin will go low. Once active, the RXRDY pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":

When 16C654 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) the TXRDY pin will go high (inactive) when the transmit FIFO is completely full. It will go low if one or more FIFO locations are empty.

Receive operation in mode "1":

When 16C654 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) and the trigger level has been reached, the RXRDY pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:

These bits are used to set the trigger level for the transmit FIFO interrupt. The 16C654 will issue a transmit empty interrupt when number of characters in FIFO drops below the selected trigger level.

BIT-5	BIT-4	FIFO Trigger Level
0	0	8
0	1	16
1	0	32
1	1	56

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO Trigger Level
0	0	8
0	1	16
1	0	56
1	1	60

LINE CONTROL REGISTER (LCR)
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR Bit 1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5, 6, 7, 8	1
1	5	1-fi
1	6, 7, 8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1= a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1=EVEN parity bit is generated by forcing an even number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR Bit-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch and Enhanced Feature mode enable (DLAB).
0=normal operation
1=Divisor latch and Enhanced Feature register enable.

MODEM CONTROL REGISTER (MCR)

This register controls the interface between the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR output to high
1=force DTR output to low

MCR BIT-1:
0=force RTS output to high
1=force RTS output to low
RTS is used as hardware flow control signal when enabled via EFR bit-6. RTS goes high when FIFO is reached to the selected trigger level and goes low as soon as content of the receive holding register is below the trigger level. Content of this register changes with state of the hardware flow control. Functions normally when hardware flow control is disabled.

MCR BIT-2:
This bit is used in internal loop-back mode only.
0=set OP1 output to high
1=set OP1 output to low

MCR BIT-3:
0=set OP2 output to high (internal loopback mode). Forces INTx outputs to three state mode if INTSEL pin is left open or connected to GND. It has no affect if INTSEL pin is connected to VCC.
1=set OP2 output to low (internal loopback mode). Sets the INTx outputs to active mode if INTSEL pin is left open or connected to GND. It has no affect if INTSEL pin is connected to VCC.

MCR BIT-4:
0=normal operating mode
1=enable local loopback mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), STS, DSR, CD and RI are disabled. Internally the transmitter output is connected to the receiver input and DTR, RTS, OP1 and OP2 are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT-5:
0= disable Xon and function, 16C550 compatible
1=enable Xon any function

MCR BIT-6:
0=standard UART receive and transmit input/output
1=infrared receive and transmit input/output. The TX A-D outputs and RX A-D inputs are converted to infrared encoder/decoder output/input format. TX output goes low when this bit is set to "1".

MCR BIT-7:
0=normal or divide by one clock input. Standard 16C550 baud rates can be selected when this bit is set to "0" and 1.8432 MHz crystal is used.
1=divide by four clock input. Standard 16C550 baud rates can be selected when this bit is set to "1" and 7.372 crystal is used.

LINE STATUS REGISTER
This register provides the status of data transfer to CPU

LSR BIT-0:
0=no data in receive holding register or FIFO
1=data has been received and saved in the receive holding register or FIFO

LCR BIT-7:
The internal baud rate counter latch and Enhanced Feature mode enable (DLAB).
0=normal operation
1=Divisor latch and Enhanced Feature register enable.

MODEM CONTROL REGISTER (MCR)

This register controls the interface between the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR output to high
1=force DTR output to low

MCR BIT-1:
0=force RTS output to high
1=force RTS output to low
RTS is used as hardware flow control signal when enabled via EFR bit-6. RTS goes high when FIFO is reached to the selected trigger level and goes low as soon as content of the receive holding register is below the trigger level. Content of this register changes with state of the hardware flow control. Functions normally when hardware flow control is disabled.

MCR BIT-2:
This bit is used in internal loop-back mode only.
0=set OP1 output to high
1=set OP1 output to low

MCR BIT-3:
0=set OP2 output to high (internal loopback mode). Forces INTx outputs to three state mode if INTSEL pin is left open or connected to GND. It has no affect if INTSEL pin is connected to VCC.
1=set OP2 output to low (internal loopback mode). Sets the INTx outputs to active mode if INTSEL pin is left open or connected to GND. It has no affect if INTSEL pin is connected to VCC.

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was emptied or if FIFO's are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
It indicates that the 16C654 is ready to accept a new character for transmission. In addition, it causes the 16C654 to issue and interrupt to the CPU when the transmit holding register empty interrupt enable is set.
0=transmit holding register is not empty
1=transmit holding register (or FIFO) is empty. CPU can load the next characters. When this bit is set, CPU can load up to 64 bytes of data to the 16C654.

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to "1" whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=normal
1=at least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS input to the 16C654 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR input to the 16C654 has changed since the last time it was read.

MSR BIT-2:
Indicates that the RI input to the 16C654 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD input to the 16C654 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loopback mode. It is the compliment of the CTS input.
CTS functions as hardware flow control signal input if it is enabled via EFR bit-7. Transmit holding register is gated with this input to start/stop the transmission. A high at this pin will stop the transmission as soon as complete character is transmitted.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loopback mode. It is the compliment of the DSR input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loopback mode. It is the compliment of the RI input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loopback mode. It is the compliment of the CD input.
Note: whenever MSR bit 3-0 is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)
16C654 provides a temporary data register to store 8 bits of information for variable use.

ENHANCED FEATURE REGISTER (EFR)
Enhanced Feature Register can be enabled/disabled via this register.

EFR BIT 0-3:
Combinations of software flow control can be selected by programming these bits.

EFR BIT-4:

Enhanced functions enable bit

0=disables the IER bits 4-5, FCR bits 4-5 and MCR bits 5-7. After hardware reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are set to "0" to be compatible with 16C550 mode.

1=enables the enhanced functions. When this bit is set to "1" all enhanced features of the 16C654 are enabled. The content of IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 can be modified and latched. After modifying the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7, the EFR bit-4 can be set to "0" to latch the contents of the new values, this feature is provided to prevent the existing software's to alter/overwrite the 16C654 enhanced functions.

HANDSHAKE CONTROL BITS

Cont-3	Cont-2	Cont-1	Cont-0	Tx, Rx software flow controls
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1 and Xon2 : Xoff1, Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1
X	X	0	1	Receiver compares Xon2, Xoff2
1	0	1	1	Transmit Xon1, Xoff1 Receiver compares Xon1, or Xon2 Xoff1 or Xoff2
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1, or Xon2 Xoff1 or Xoff2
1	1	1	1	Transmit Xon1 and Xon2 : Xoff1, Xoff2 Receiver compares Xon1 and Xon2 : Xoff1, Xoff2
0	0	1	1	No transmit flow control Receiver compares Xon1 and Xon2 : Xoff1, Xoff2

EFR BIT-5

0=normal
1=special character detect
16C654 compares the incoming receive data with Xoff-2 data. Upon correct match, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character.

EFR BIT-6:

RTS flow control
0=normal. RTS flow control is disabled. Standard 16C550 mode.
1=RTS pin goes high when receive FIFO's reach the programmed trigger level.

EFR BIT-7:
CTS flow control
0= normal. CTS flow control mode is disabled. Standard 16C550 mode.
1=transmission is resumed when low input signal is detected on the CTS pin.

FIFO READY REGISTER
This register provides the state of the transmit and receive FIFO.

FIFORdy BIT 0-3:
0=transmit FIFO is full. The 16C654 can not take any more transmit data.
1=one or more empty locations in FIFO is below transmit trigger level.

FIFORdy BIT 4-7:
0=receiver is above the trigger level or time-out has occurred.
1=receiver is not ready

16C654 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	EFR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0; LSR BITS 5-6=1; LSR BIT-7=0
MSR	MSR BITS 0-3=0; MSR BITS 4-7=INPUT SIGNALS
FCR	FCR BITS 0-7=0
EFR	EFR BITS 0-7=0

SIGNALS	RESET STATE
TX A-D	High
RTS A-D	High
DTR A-D	High
RXRDY A-D	High
TXRDY A-D	Low