Introduction

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If this default configuration is suitable for y
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Introduction

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If this default configuration is suitable for your application, you may proceed to Chapter 3. Otherwise, read Chapter 2 for setup information.

– Note –

Configuring your BlackBoard-8/650

Selecting a Starting address:

Each port (16650 UART) on the BlackBoard-8/650 occupies 8 bytes of I/O. Since there are 8 16650 UARTS on the BlackBoard-8/650, each card occupies 64 bytes of I/O space on your computer. Each port on your BlackBoard-8/650 must have an address associated with it. Your BBS software needs to know the address for each port in order to send and receive data to and from the UART.

Your BBS software allows you to specify the I/O address and interrupt for each port. You must first determine where you have an available range of I/O space (64 addresses or more) in your computer. I/O space on the PC/XT machines occupies 0–3FFh. Some of the I/O space is already used by the PC as shown in the following I/O Map. Remember that PC/XT/AT's use 10 bit I/O addressing allowing for I/O in the range of 0–3FFh. Adresses at or above 400h are redundant unless the adapter card decodes A10 through A15 when determining its I/O address.

Hex Range	Usage
000–00F	8237 Direct Memory Access Controller #1
020–021	8259 Programmable Interrupt Controller #1
040–043	8253 Timer
060–063	8255 PPI (XT)
060–064	8742 Controller (AT keyboard)
070–071	CMOS Ram & NMI Mask Register (AT)
080–08F	DMA Page Registers
0A0–0A1	8259 PIC #2 (AT)
0A0–0AF	NMI Mask Register (XT)
0C0–0DF	8237 DMA #2 (AT–Word Mapped)
0F0–0FF	80287 Numeric CoProcessor (AT)
100–107	PS/2 type programmable option select registers
1F0–1FF	Hard Disk (AT)
200–20F	Game/Control Port
210–21F	Expansion Unit (XT)
238–23B	Bus Mouse
23C–23F	Alternate Bus Mouse
278–27F	Parallel printer
Hex Range	Usage
2B0–2BF	EGA Display Port
2C0–2CF	EGA Display Port (alt)
2D0–2DF	EGA Display Port (alt)
2E0–2E7	GPIB (AT)
2E8–2EF	Serial Port (COM4)
2F8–2FF	Serial Port (COM2)
300–30F	Prototype Card
310–31F	Prototype Card
320–32F	Hard Disk (XT)
378–37F	Parallel Printer
380–38F	SDLC
3A0–3AF	SDLC
3B0–3BB	MDA
3BC–3BF	Parallel Printer
3C0–3CF	EGA
3D0–3DF	CGA
3E8–3EF	Serial Port (COM3)
3F0–3F7	Floppy Disk
3F8–3FF	Serial Port (COM1)

If you are not sure about which address range is available on your PC, run the program "IOMAP.EXE" which is supplied on your BlackBoard-8/650 Support Software disk. This program will give you a visual "snapshot" of the I/O space in the 100–3FF range. You will then be able to determine which I/O addresses are in use by another device.

The following address and interrupt modes are available on the standard BlackBoard-8/650. Other custom modes are available. Contact GTEK for more details.

Addressing Modes

JP1 0	JP1 1	JP1 2	Port 0	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Status	Mode
—	0	0	200	600	A00	E00	1200	1600	1A00	1E00	207	Vertical Addressing Mode #1
0	0	0	210	610	A10	E10	1210	1610	1A10	1E10	217	Vertical Addressing Mode #2
0	—	0	100	108	110	118	120	128	130	138	107	Mode #1
0	0	—	140	148	150	158	160	168	170	178	147	Mode #2
—	—	0	180	188	190	198	1A0	1A8	1B0	1B8	187	Mode #3
0	—	—	280	288	290	298	2A0	2A8	2B0	2B8	287	Mode #4
—	0	—	2C0	2C8	2D0	2D8	2E0	2E8	2F0	2F8	2C7	Mode #5
—	—	—	2C0	2C8	2D0	2D8	3E8	2E8	3F8	2F8	2C7	COMM 1234
Discrete IRQ port assignments			10	11	12	15	5	7	4	3	See Chart at end of this chapter	

0 = Jumper installed, — = NO Jumper installed.

Note when you use the COMM1234 mode above, you obtain COM1 on port 6, COM2 on port 7, COM3 on port 4 and COM4 on port 5.

A Word About Interrupts

Not all BBS software uses interrupts for its serial communication. If your software does not use interrupts for serial data, set jumpers as seen above. If your software requires interrupts for serial comunication, please read on...

In addition to knowing where the UARTs are, your software needs to know which ports are associated with each interrupt. This is so that when the PC receives an interrupt request on a certain IRQ line, it knows from where the interrupt came.

Some software requires that each port on your BlackBoard-8/650 has a dedicated interrupt. Other BBS software (TBBS for example) allows you to assign all ports to only one interrupt. if your software allows interrupt sharing, you should probably use it. Interrupt sharing conserves interrupts and allows them to be used for other devices, eg. CD Roms, Hard Disk Drives, Parallel Ports, etc.

First, you must determine how many interrupts you will need for your BBS software. (Ask your software Vendor about this.) Then figure out which interrupts are available to you in your PC. As with I/O address space, certain interrupts are already used by your PC and may not be used by your BlackBoard-8/650. See the following chart and then see the table following for interrupt selections.

Common Hardware Interrupts used by an AT class computer:

Name	Description
NMI	Parity (not available on bus)
0	Timer (not available on bus)
1	Keyboard (not available on bus)
2	Cascade
3	COM or SDLC
4	COM or SDLC
5	LPT (XT = Hard Disk)
6	Floppy Disk
7	LPT
8	Real Time Clock
9	Re-Directed to IRQ2
10	Unassigned
11	Unassigned
12	Unassigned
13	80x87 Coprocessor
14	Hard Disk
15	Unassigned

Interrupt Modes

Shared IRQs

To share IRQs: Select channels to be shared by placing a jumper corresponding to the port # on JB6 that you wish to share. Place a jumper on JB7 in the desired IRQ position to select which IRQ will be shared.

Discrete IRQs

For discrete IRQs, jumper the two pins between JB6 and JB7 as shown in the chart at the end of the chapter.

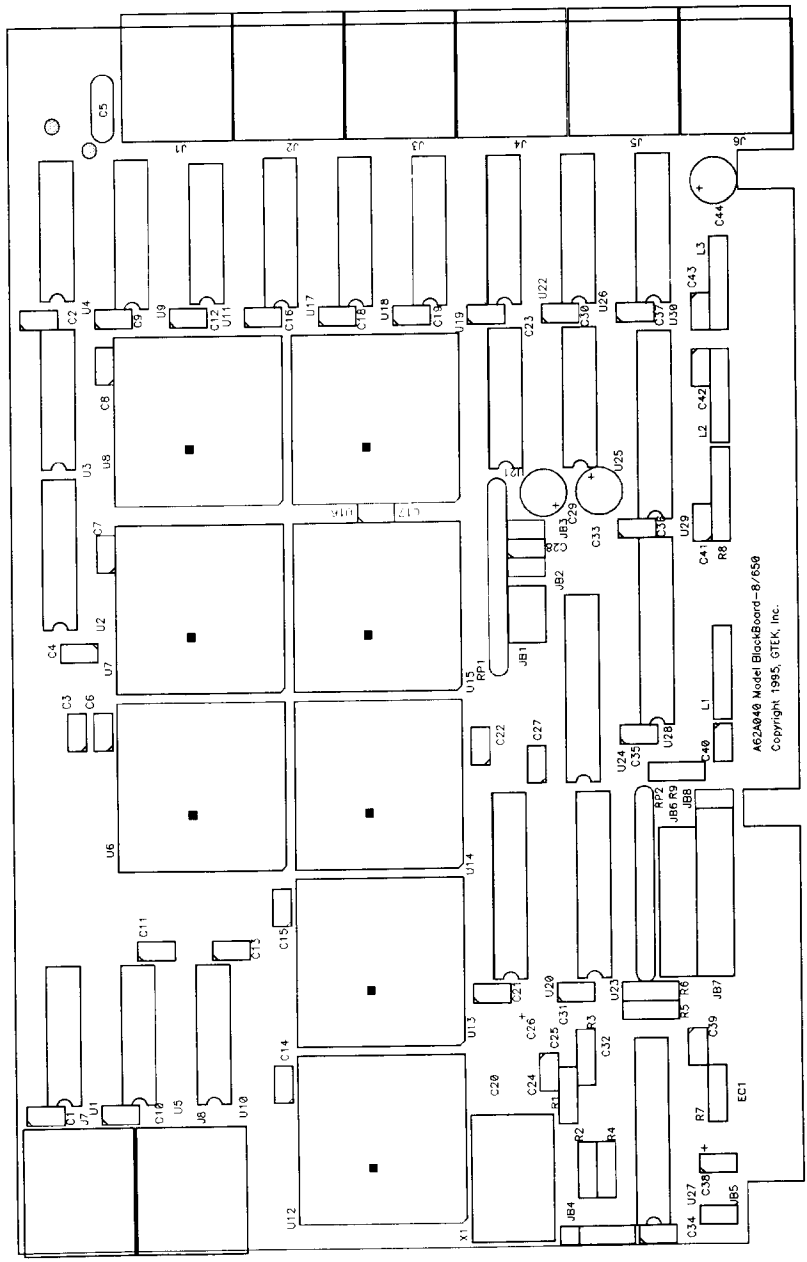
No IRQs

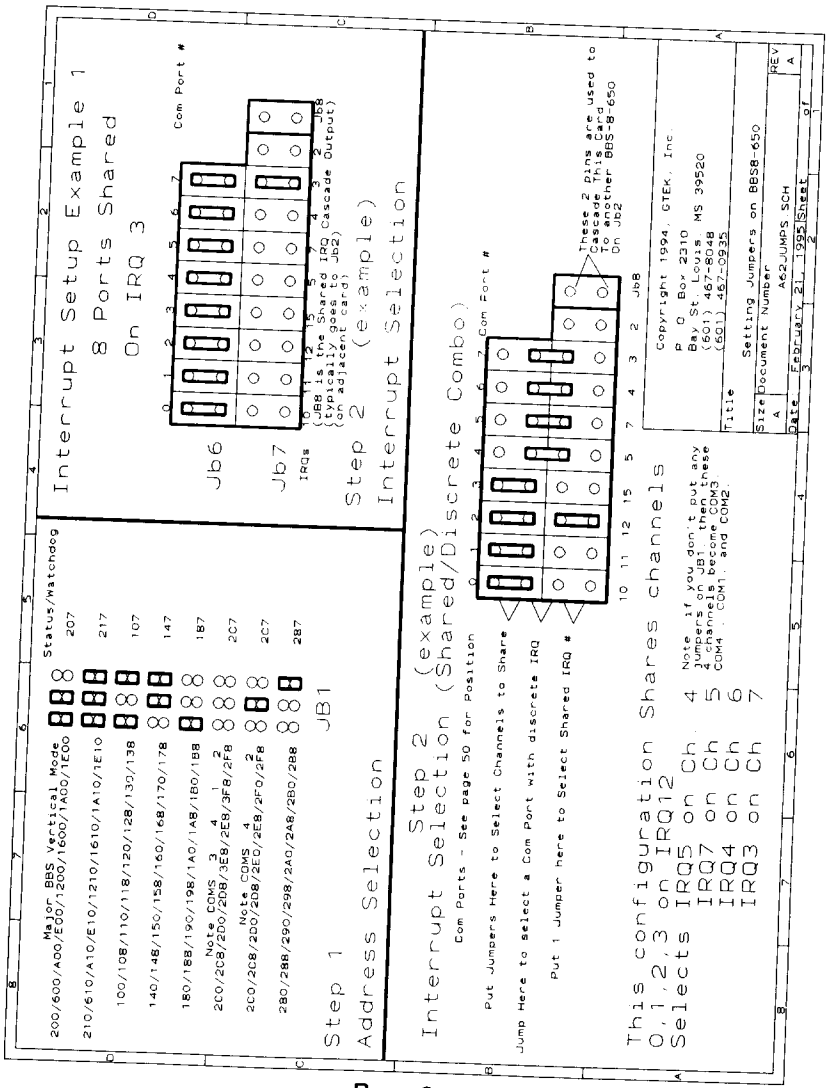
To use NO IRQs on one or more channels simply do not place a jumper on a particular channel (JB6, 1 through 8).

To Cascade Boards:

To share an IRQ across BlackBoard-8/650's, you have to place a jumper on JB8 (output on the first card in the series) to JB2 (input on the second card of the series). Likewise if there are more than 2 cards you are cascading, keep running JB8 to JB2 from one card to the other. The jumper is polarized so that the active pin is UP. A single wire is all that is required for this pin on JB2 and JB8, but it has to be the TOP pin. **CAUTION: If you are not cascading cards, JB2 MUST REMAIN JUMPERED (covered).**

Don't forget to select an addressing mode on each card with JB1 pins 1,2 and 3 that is compatible with all the cascaded boards.


A62A040 Model BlackBoard-8/650
Copyright 1995, GTEK, Inc.


Step 1
Address Selection
Major BBS Vertical Mode
Status/Watchdog
200/600/A00/E00/1200/1600/1A00/1E00 207
210/610/A10/E10/1210/1610/1A10/1E10 217
100/108/110/118/120/128/130/138 107
140/148/150/158/160/168/170/178 147
180/188/190/198/1A0/1A8/1B0/1B8 187
Note COMS 3 4 1 2
2C0/2C8/2D0/2D8/3E8/2E8/3F8/2F8 2C7
Note COMS 4 2
2C0/2C8/2D0/2D8/2E0/2E8/2F0/2F8 2C7
280/288/290/298/2A0/2A8/2B0/2B8 287
JB1
Interrupt Selection (examples)
Com Ports - See page 50 for Position
Put Jumpers Here to Select Channels to Share
Jump Here to Select a Com Port with discrete IRQ
Put 1 Jumper here to Select Shared IRQ #
This configuration Shares channels
0,1,2,3 on IRQ12
Selects IRQ5 on Ch 4
IRQ7 on Ch 5
IRQ4 on Ch 6
IRQ3 on Ch 7
Note if you don't put any jumpers on JB1, then these 4 channels become COM3 COM4 . COM1 and COM2
Step 2 (examples)
Interrupt Selection (Shared/Discrete Combo)
Com Port #
Jb6
Jb7
IRQs
JB8 is the Shared IRQ Cascade Output (typically goes to Jb2) (on adjacent card)
Step 2 (example)
Interrupt Selection
Interrupt Setup Example 1
8 Ports Shared
On IRQ 3
Com Port #
JB8
These 2 pins are used to Cascade This Card On Jb2 Another BBS-8-650
JB8
Copyright 1994, GTEK, Inc
P O Box 2310
Bay St Louis MS 39520
(601) 467-8048
(601) 467-0935
Title
Setting Jumpers on BBS8-650
Size
Document Number
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Date
February 21, 1995
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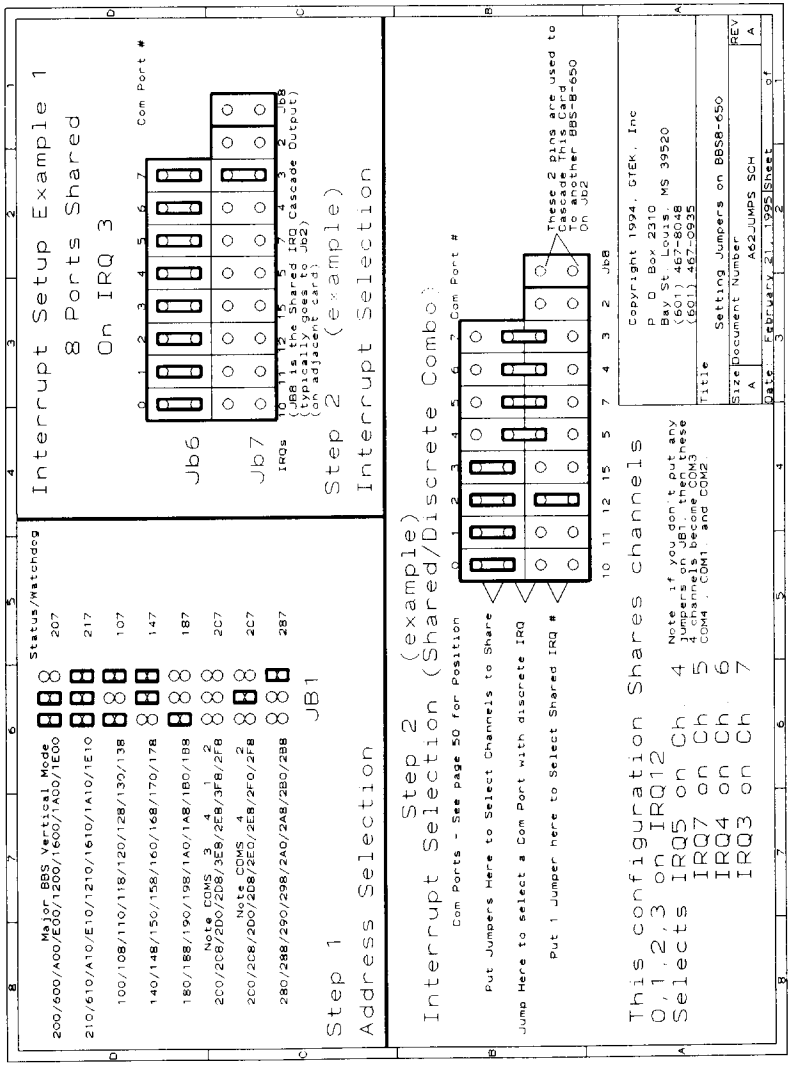
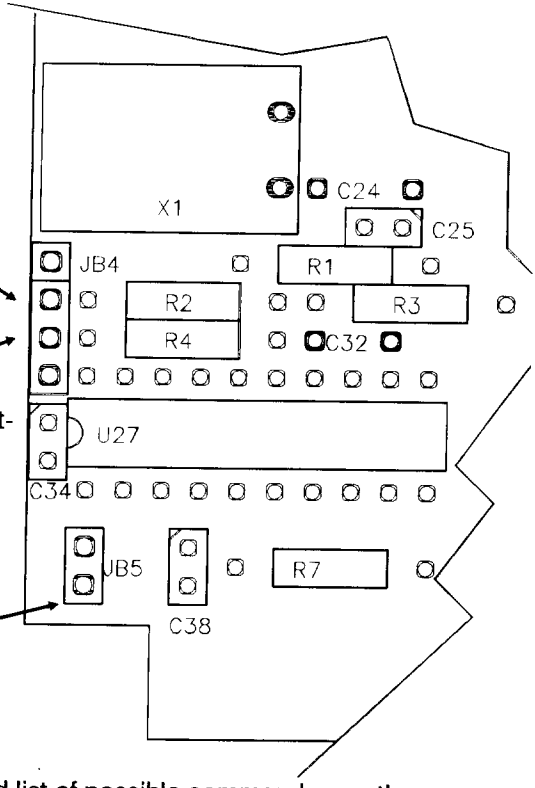
of
3


Step 1
Address Selection
Major BBS Vertical Mode
200/600/A00/E00/1200/1600/1A00/1E00
210/610/A10/E10/1210/1610/1A10/1E10
100/108/110/118/120/128/130/138
140/148/150/158/160/168/170/178
180/188/190/198/1A0/1A8/1B0/1B8
200/208/200/208/3E8/2E8/3F8/2F8
280/288/290/298/2A0/2A8/2B0/2B8
Status/Watchdog
207
217
107
147
187
207
207
287
JB1
Step 2 (example)
Interrupt Selection
Com Ports - See page 50 for Position
Put Jumpers Here to Select Channels to Share
Jump Here to select a Com Port with discrete IRQ
Put 1 Jumper here to Select Shared IRQ #
This configuration Shares channels
0,1,2,3 on IRQ12
Selects IRQ5 on Ch 4
IRQ7 on Ch 5
IRQ4 on Ch 6
IRQ3 on Ch 7
Note if you don't put any
jumpers in JB8 then these
4 channels become COM3
COM4 , COM1 and COM2
Interrupt Setup Example 1
8 Ports Shared
On IRQ 3
Com Port #
Jb6
Jb7
IRQs
JB8 is the Shared IRQ Cascade Output)
(To daisy chain boards JB2)
(or adjacent boards)
Step 2 (example)
Interrupt Selection
Com Port #
Jb8
These 2 pins are used to
Cascade This Card
To another BBS-B-650
On JB2
Copyright 1994, GTEK, Inc
P O Box 2310
Bay St Louis, MS 39520
(601) 467-8048
(601) 467-9935
Title
Setting Jumpers on BBS8-650
Size
A
Document Number
A62JUMPS SCH
REV
A
Date: February 21, 1995 Sheet 2 of

To connect Guardian Watchdog(tm) system to your computer, Plug supplied Jumper onto the Top Two Pins of JB4 and plug the other end onto your motherboard where you unplugged your reset pushbutton



Plug your reset pushbutton that you removed from your motherboard onto the Bottom Two Pins of JB4.

DO NOT plug anything onto JB5!

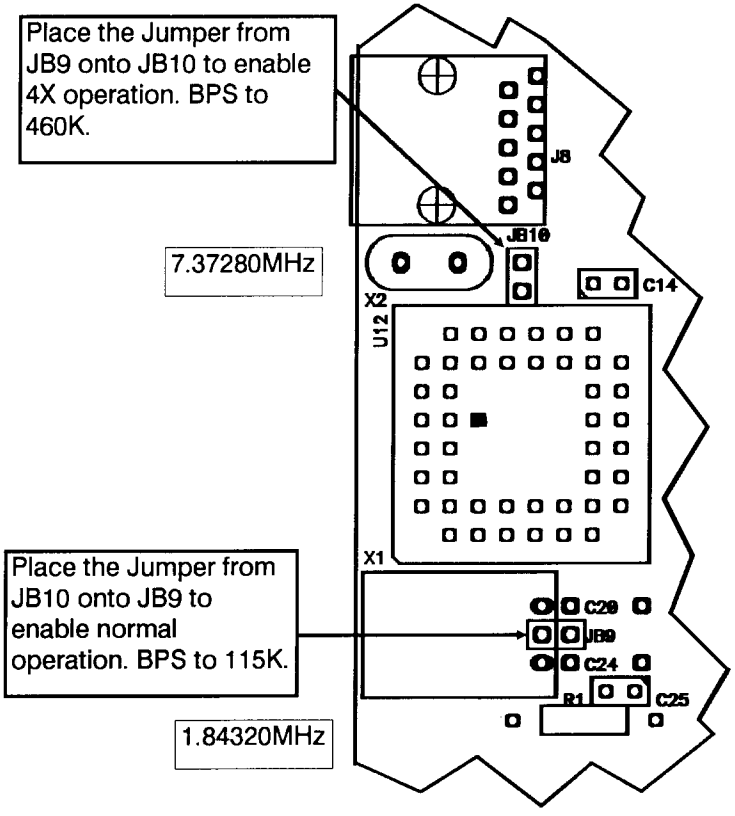
To get a help screen and list of possible commands, run the watchdog program without parameters:

```
WDOG ADDR
Where {100,140,180,200,210,280,2C0,2C0 } allow-
able addresses
wdog addr D {disable after install as above}
wdog addr R {re-enable after disable above}
If WDOG ADDR R is done before WDOG ADDR, then com-
puter may reset if Guardian Watchdog is connected.
```

–NOTES–

Enabling High Speed Operation

This picture/feature applies ONLY to Revision–A boards or later.



Physical Installation

After you have selected the base address and interrupt mode for your BlackBoard-8/650, you may proceed with the physical installation of the card. You may wish to make a note of you current jumper settings for future use.

CAUTION:

Be sure that the power is off and the power cord is removed from the PC before installing or proceeding with the installation.

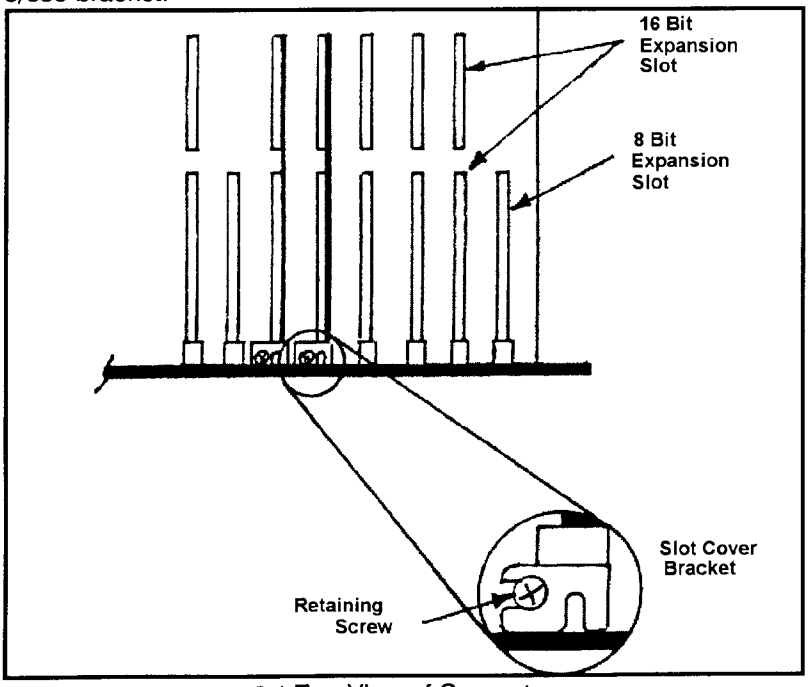
You may wish to consult with your computer's owner manual about installation of expansion cards. If you are not familiar with the process of installing expansion cards in your computer or if you feel uncomfortable with this installation, refer the installation to qualified personnel. Failure to follow these instructions may result in damage to your computer, damage to the BlackBoard-8/650 or both.

Step 1 – Carefully remove the cover of your PC.

Case styles vary, so follow the instructions in your computer manual for removing the cover of your PC to expose the expansion slots.

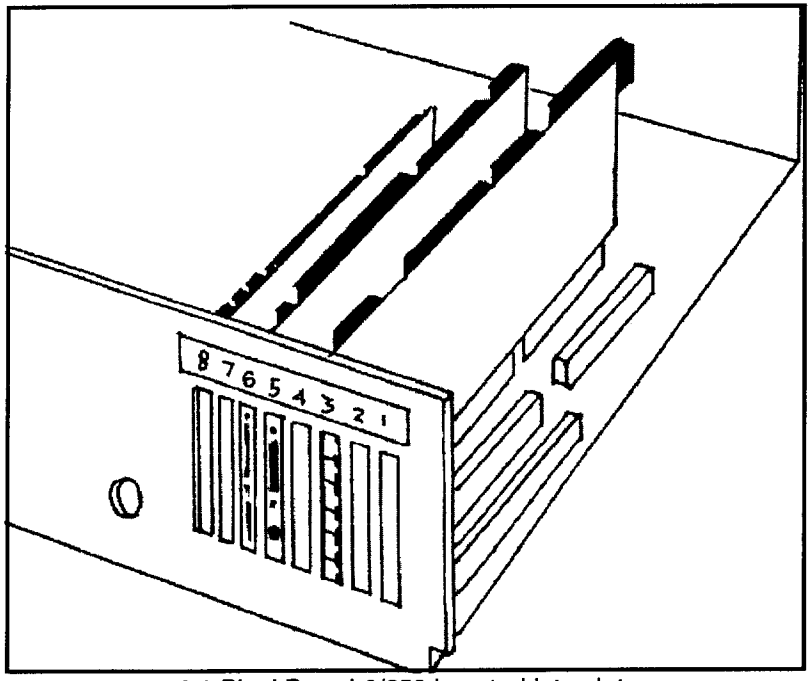
Step 2 – Choose an available 8 or 16 bit expansion slot.

Eight bit slots will have only one card edge connector, and 16 bit slots will have 2 card edge connectors. In order to access the higher (above IRQ7) interrupts, you will have to install your BlackBoard-8/650 in a 16 bit slot. You will need to remove the screw and bracket which covers the slot hole. Retain the screw for the BlackBoard-8/650 bracket.



3.1 Top View of Computer

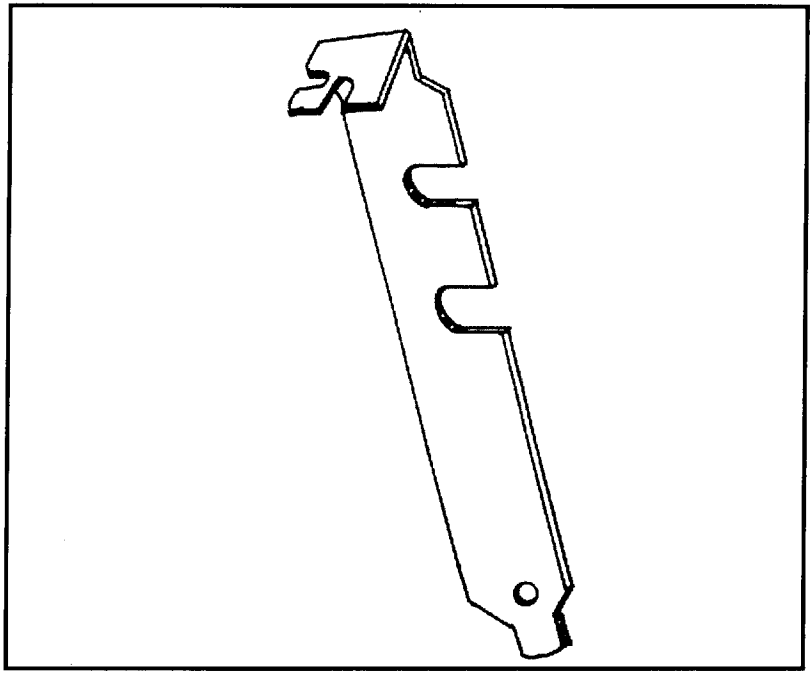
Step 3 – Carefully insert the BlackBoard-8/650 into the available slot and secure it in place with the screw you removed from step 2.



3.2 BlackBoard-8/650 inserted into slot.

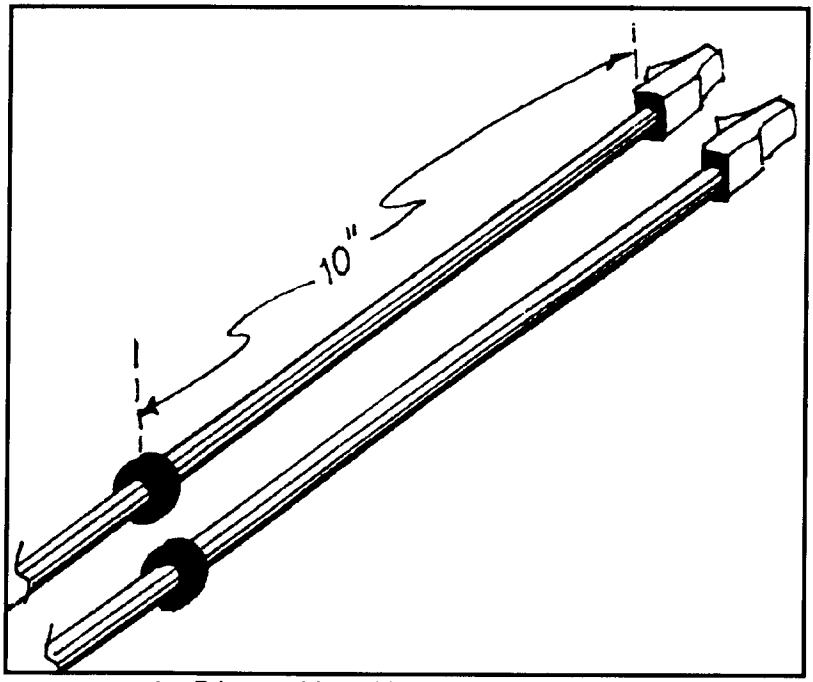
Step 4 -- Insert cable retaining bracket.

If you will be using the two ports on the rear of the BlackBoard-8/650 (Ports 6 & 7), you may wish to use the cable retaining bracket supplied with the unit. The cable retaining bracket has 2 cutouts which are made to accomodate the 2 cables which plug into ports 6 & 7.



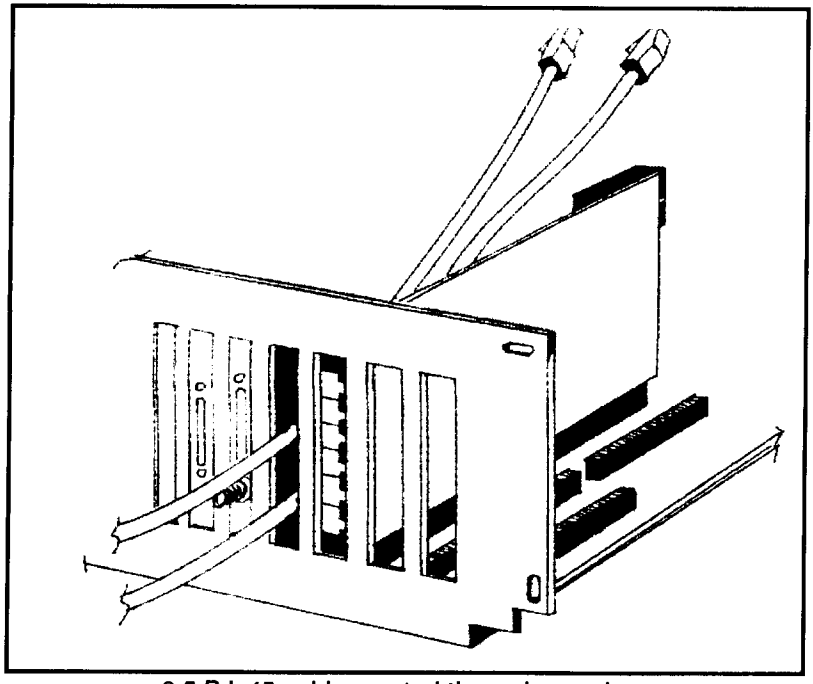
3.3 Cable retaining bracket.

The 2 cables for ports 6 & 7 can be indentified by the rubber grommets which are installed approximately 10 inches from the RJ–45 plug.



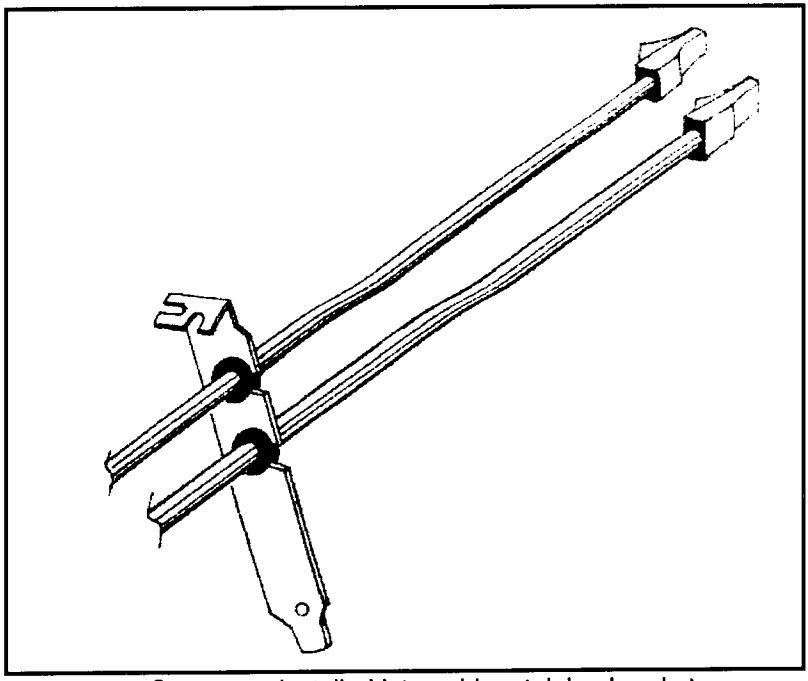
3.4 RJ–45 cables with rubber grommets (2).

To install the cable retaining bracket, first remove an existing cover bracket and retain the screw. Locate the cables for ports 6 & 7 and then carefully route the cables through the slot where you removed the existing cover.



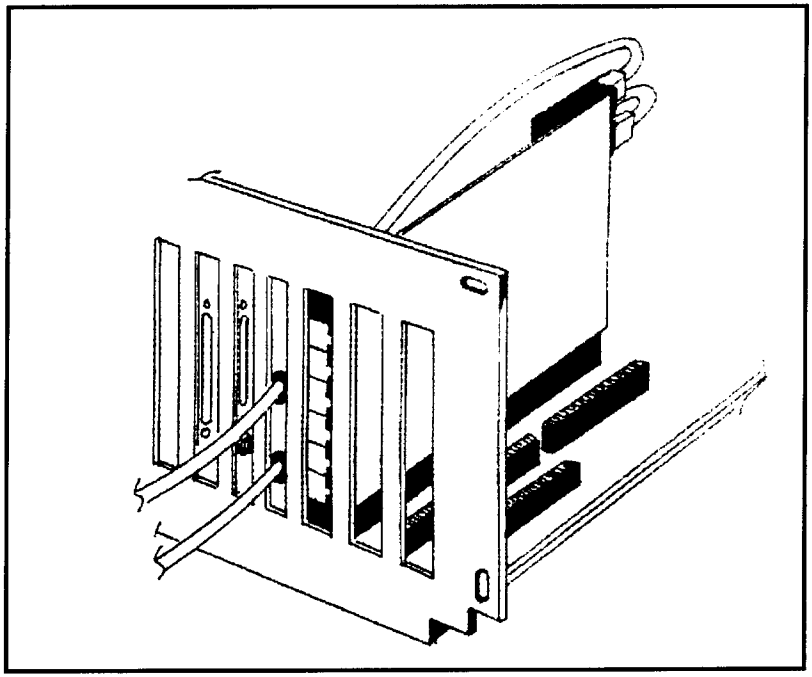
3.5 RJ–45 cables routed through opening.

Insert the rubber grommets into the slots on the retaining bracket and secure it with the screw.



3.6 Grommets installed into cable retaining bracket.

You may then plug these cables into the two RJ–45 connectors on the rear of the BlackBoard-8/650. Channel 6 is on top and Channel 7 is next.



3.7 BlackBoard-8/650 installed into computer.

–NOTES–

4 – SOFTWARE LICENSE AGREEMENT

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5 – LIMITED WARRANTY

5.1 HARDWARE

GTEK, INC., warrants to the original purchaser of this GTEK, INC., product that it is to be in good working order for a period of one year from the date of purchase from GTEK, INC., or an authorized GTEK, INC., dealer. Should this product, in GTEK, INC.'s opinion, malfunction during the warranty period, GTEK will, at its option, repair or replace it at no charge, provided that the product has not been subjected to misuse, abuse, or non-GTEK authorized alterations, modifications, and / or repairs.

Products requiring Limited Warranty service during the warranty period should be delivered to GTEK with proof of purchase. If the delivery is by mail, you agree to insure the product or assume the risk of loss or damage in transit. You also agree to prepay the shipping charges to GTEK.

All Express And Implied Warranties For This Product Including, But Not Limited To, The Warranties Of Merchantability And Fitness For A Particular Purpose, Are Limited In Duration To The Above 1 Year Period. Some states do not allow limitations on how long an implied warranty lasts, so the above limitations may not apply to you.

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This Warranty Gives You Specific Legal Rights, And You May Also Have Other Rights Which May Vary From State To State.

The limited warranty applies to hardware products only.

5.2 SOFTWARE

This Product Is Not A Consumer Product Within The Meaning Of The Uniform Commercial Code And Applicable State Law. The Program Is Provided "AS IS" Without Warranty Of Any Kind, Either Expressed Or Implied, Including, But Not Limited To The Implied Warranties Of Merchantability And Fitness For A Particular Purpose. The Entire Risk As To The Quality And Performance Of The Program Is With You. Should The Program Prove Defective, You (Not GTEK, INC.) Assume The Entire Cost Of All Necessary Servicing, Repair Or Correction. Some States Do Not Allow The Exclusion Of Implied Warranties, So The Above Exclusion May Not Apply To You. This Warranty Gives You Specific Legal Rights And You May Also Have Other Rights Which Vary From State To State.

GTEK, Inc. does not warrant that the functions contained in the program will meet your requirements or that the operation of the program will be uninterrupted or error free. However, GTEK, Inc. warrants the diskette(s) on which the program is furnished, to be free from defects in materials and workmanship under normal use for a period of ninety (90) days from date of delivery to you as evidenced by a copy of your receipt.

Licensee herein acknowledges that the software licensed hereunder is of the class which inherently cannot be tested against all contingencies by Licensor. Licensee acknowledges Licensee's obligation to test all programs produced by the licensed software to determine suitability and correctness prior to use.

5.3 LIMITATIONS OF REMEDIES

GTEK, Inc.'s entire liability and your exclusive remedy shall be:
1. the replacement of any diskette(s) not meeting GTEK's "Limited Warranty" and which is returned to GTEK, Inc. with a copy of your receipt, or
2. if GTEK, Inc. or the dealer is unable to deliver a replacement diskette(s) which is free of defects in materials or workmanship, you may terminate this Agreement by returning the program and your money will be refunded.

In No Event Will GTEK, INC. Be Liable To You For Any Damages, Including Any Lost Profits, Lost Savings Or Other Incidental Or Consequential Damages Arising Out Of The Use Or Inability To Use Such Program Even If GTEK, INC. Has Been Advised Of The Possibility Of Such Damages, Or For Any Claim By Any Other Party.

Some States Do Not Allow The Limitation Or Exclusion Of Liability For Incidental Or Consequential Damages So The Above Limitation Or Exclusion May Not Apply To You.

5.4 GENERAL

You may not substitute, assign or transfer the license or the program except as expressly provided in this Agreement. Any attempt otherwise to sublicense, assign or transfer any of the rights, duties or obligations hereunder is void.

This Agreement will be governed by the laws of the State of Mississippi.

Should you have any questions concerning this Agreement, you may contact GTEK, Inc. by writing to:

GTEK, Inc. Sales and Service
P. O. Box 2310
Bay St. Louis, MS 39521–2310

— Notes —

6 – SERVICE

For warranty service or non warranty service, contact GTEK, INC. at (601) 467–8048 to obtain an RMA (Return of Material Authorization number). We will need the serial number and date of purchase. Send the BBS550, freight prepaid to:

GTEK, INC.
RMA #####
399 Highway 90
Bay St. Louis, MS. 39520

Be sure to include the RMA number on and in the package so we will know what to do with it. Out of warranty service charges are determined on an hourly labor plus materials basis.

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Information to user: The user is cautioned that changes or modifications not expressly approved by GTEK, Inc. could void the user's authority to operate the equipment.

– NOTE –

16650 Technical Reference

The 32 byte data FIFO's are enabled when the user writes to the control register. The 16650 provides independent trigger levels for both receiver and transmitter. To be compatible with the 16550, the 16 byte transmit trigger level is selected after reset. Note that the user can write to transmit trigger levels but activation will not take place until the 16650 special mode is selected (EFR bit-4 is set to "1").

The contents of the Xon-1,2, and Xoff 1,2 are not reset to any given values and user can write any values desired for software flow controls. Different conditions can be set to detect Xon/Xoff characters or start/stop the transmissions. See the table for all possible conditions. When single Xon/Xoff characters are selected, the 16650 compares the incoming data with these values and controls the transmission, these characters are not stacked in data buffer or FIFO. Special case is provided to detect the special characters and stack it into the data buffer or FIFO. These conditions are selected via Enhanced Feature Register (EFR bit 0 - 3).

Hardware flow control can be selected when either or both bits of the EFR bit 6-7 are set to "1". When auto CTS is selected, the 16650 will stop the transmission as soon as a complete character is transmitted and CTS input level is high. Transmission is resumed after CTS input changes to low level.

RTS pin will be forced to high state regardless of it's original state when receive FIFO reaches to the programmed trigger level. RTS pin resumes its original state after content of the data buffer (FIFO) drops below the programmed trigger level. Both hardware and software flow controls can be enabled for automatic operation. During these conditions,

the 16650 will accept additional data to fill the unused transmit and receive FIFO locations.

When EFR bit-4 and IER bit-4 are set to "1", the 16650 enters into sleep mode and resumes it's normal operation when a data is received or state of the modem input pins changes or it is set to transmit data. This mode is active until disabled.

Special care should be considered for the following interrupt conditions and handling them. After reset, if the transmitter interrupt is enabled, the 16650 will issue an interrupt to indicate that transmit holding register is empty, no other interrupts will be issued after enabling the interrupt. The LSR register has highest interrupt priority and CTS, RTS have lowest interrupt priority. The interrupt status register will show the highest interrupt priority condition, and after servicing the interrupt condition next priority interrupt level will be shown. There are two interrupt conditions that have the same priority and it is important to know the conditions to service. Receive data ready and receive time out share the same priority with one additional bit (IER bit-3). Receiver issues interrupt after number of characters have reached the programmed trigger level, in this case, the 16650 holds equal or more characters that the trigger level. After reading a block of data, the user can check the LSR bit-0 for additional characters. If the number of characters in the receive data register did not reach the programmed trigger level within a certain time frame, the 16650 will issue receive data ready interrupt with ISR bit-3 set to "1".

Note that the receive time out is functional only in the 650 mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or at the time the receive holding register is read. The actual time out value is T (time out length in bits) = 4 x P (programmed word length) +12. To convert time out value to a character value, user has to divide

this number to its complete word length + parity (if used) + number of stop bits and start bit.

Due to the number of active simultaneous interrupt limitations in PC's , the 16650 offers shared interrupt out by setting MCR bit-5 to "1".

A dual baud rate generator is provided to maintain the 16550 compatibility and provide higher data rate when it is needed. The 16550 and the 16650 baud rate generator tables can be selected by setting/resetting the MCR bit-7.

The 16650 transmit trigger level provides additional flexibility to the user for block mode operation. In 16550/650 mode, LSR bits 5-6 give indication whether the transmitter is empty or not. There is not mechanism to identify FIFO full state or available empty locations in FIFO. User can select one of the two possible ways to operate the transmit and receive FIFO by utilizing the DMA mode (FAR bit-3). When FIFO's are enabled and DMA mode "0" is selected, the 16650 sets the interrupt bit and activates interrupt output pin for single transmit and receive operation like the 16450 mode except that it can receive and transmit 32 bytes of characters. When DMA mode "1" is activated, the user can take advantage of the block mode operation. In this mode, transmitter /receiver sets the interrupt flag and interrupt output pin, when characters in the FIFO are below the transmit trigger level or over receive trigger level. Since the 16550 does not have transmit trigger levels, the default trigger level in the 16650 is set to 16 bytes (trigger level "0").

A2	A1	A0	Read Mode	Write Mode
0	0	0	Receive Holding Register	Transmit holding register
0	0	1		Interrupt enable register
0	1	0	Interrupt Status Register	FIFO control register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	***0***	***0***	***LSB of Divisor Latch***	***LSB of Divisor Latch***
0	***0***	***1***	***MSB of Divisor Latch***	***MSB of Divisor Latch***
0	***1***	***0***	***Enhanced Feature Register***	***Enhanced Feature Register***
1	***0***	***0***	***Xon-1 Word***	***Xon-1 Word***
1	***0***	***1***	***Xon-2 Word***	***Xon-2 Word***
1	***1***	***0***	***Xoff-1 Word***	***Xoff-1 Word***
1	***1***	***1***	***Xoff-2 Word***	***Xoff-2 Word***

Bold Registers are accessible only when LCR bit-7 is set to "1".

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of the data bus (D7 - D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0 = 1) and receive interrupts (IER Bit-0 = 1)are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0 = 1; resetting IER BIT 3-0 to zero puts the 16650 in the FIFO polled mode of operation. Since the receiver and the transmitter are controlled separately either one or both can be in the polled mode of operation by utilizing the Line Status Register.

A) LSR Bit-0 will be set as long as there is one byte in the receive FIFO.

B) LSR Bit 4-1 will specify which error(s) have occurred.

C) LSR Bit-5 will indicate when the transmit FIFO is empty.

D) LSR Bit-6 will indicate when both transmit FIFO and transmit shift registers are empty.

E) LSR Bit-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR

The 16650 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC - 24 MHz and dividing it by any divisor form 1 to 2^{16} -1. The output frequency of the Baud-out* is equal to 16X of the transmission baud rate (Baud-out*=16 x Baud Rate). Customized Baud rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

BAUD RATE GENERATOR PROGRAMMING TABLE (7.372 MHz CLOCK):

Baud Rate MCR BIT-7 = 1 (see note)	*Baud Rate MCR Bit-7 = 0*	*16 x CLOCK DIVISOR "Decimal"*
50	200	2304
75	300	1536
150	600	768
300	1200	384
600	2400	192
1200	4800	96
2400	9600	48
4800	19.2K	24
7200	28.8K	16
9600	38.4K	12
19.2K	76.8K	6
38.4K	153.6K	3
57.6K	230.4K	2
115.2K	460.8K	1

Note: These are the baud rates with an 1.8432 MHz crystal and MCR bit 7=0

HARDWARE FLOW CONTROL OPERATION.

When hardware flow control operation is enabled, the 16650 monitors the CTS* pin for transmit operation and receiver trigger level for RTS* operation. When CTS* changes state from low to high, the 16650 suspends the transmission operation as soon as a complete character is transmitted. ISR bit-5 will be set (if enabled via IER bit 6-7). Transmission will resume as soon as CTS* pin goes low. RTS* pin will be forced to high state when receiver FIFO reaches the programmed trigger level. RTS* will go low when Receive Holding Register is below the next lower trigger level. The 16650 will accept additional data when transmission is suspended during hardware flow control until all locations are filled.

SOFTWARE FLOW CONTROL

When software flow control operation is enabled, the 16650 will compare the two sequential received data bytes with Xoff-1,2 programmed characters. When these characters match, the 16650 will halt the transmission after finishing the transmission of the complete character. The receive ready, Xoff (if enabled via IER bit-5) flags will be set and the interrupt output pin (if receive interrupt is enabled) will be activated. After the recognition of the Xoff characters, the 16650 will compare the next two incoming characters with Xon-1,2 characters. The 16650 will resume the operation and clear the flags (ISR bit-4) when Xon characters are received. The 16650 will send Xoff-1,2 characters as soon as received data passed the programmed trigger level. The 16650 will transmit programmed Xon-1,2 characters as soon as receive data has reached to the next lower trigger level.

INTERRUPT ENABLE REGISTER (IER)

The interrupt enable register (IER) masks the incoming

interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0 = Disable the receiver ready interrupt.
1 = Enable the receiver ready interrupt.

IER BIT-1:
0 = Disable the transmitter empty interrupt.
1 = Enable the transmitter empty interrupt.

IER BIT-2:
0 = Disable the receiver line status interrupt.
1 = Enable the receiver line status interrupt.

IER BIT-3:
0 = Disable the modem status register interrupt.
1 = Enable the modem status register interrupt.

IER BIT-4:
0 = Disable sleep mode.
1 = Enable sleep mode. The 16650 enters into power down mode and external clock or oscillator circuit is disabled. Any change of state on the RX, RI*, CTS*, DSR*, and CD* pins start the 16650. The 16650 will not lose the programmed bits when sleep mode is activated or deactivated. The 16650 will not enter in sleep mode if any interrupt is pending.

IER BIT-5:
0=Disable the received Xoff interrupt.
1 = Enable the received Xoff interrupt. The 16650 issues an interrupt when Xoff characters are received and correctly match the Xoff 1,2 words.

IER Bit-6:

0 = Disable the RTS interrupt.

1 = Enable the RTS interrupt. The 16650 issues and interrupt when the RTS pin changes state from low to high.

IER BIT-7:
0 = Disable the CTS interrupt.
1 = Enable the CTS interrupt. The 16650 issues an interrupt when the CTS pin changes state from low to high.

INTERRUPT STATUS REGISTER (ISR)

The 16650 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The interrupt status register (ISR) provides the sources of the interrupt in a prioritized matter. During the read cycle, the 16650 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt is

P	D5	D4	D3	D2	D1	D0	Source of the interrupt
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY (Received Data Ready)
2	0	0	1	1	0	0	RXRDY (Receive Data Time Out)
3	0	0	0	0	1	0	TXRDY (Transmit Holding Register Empty)
4	0	0	0	0	0	0	MSR (Modem Status Register)
5	0	1	0	0	0	0	RXRDY (Received Xoff signal) / Special character
6	1	0	0	0	0	0	CTS, RTS change of state

ISR Bit - 0:
0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1 = no interrupt pending.

ISR Bit 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR Bit 4 - 5:
Thses bits are enabled when the FER bit-1 is set to "1". ISR bit-4 indicates that matching Xoff characters have been detected. ISR bit-5 indicates that CTS, RTS have been received or issued. Note that the ISR bit-4 will stay "1" until Xon characters are received.

ISR Bit 6-7:
These bits are not used and are set to zero in the 16450 mode. Bits 6-7 are set to "1" in the 16650 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR Bit-0:
0 = Disable the transmit and receive FIFO.
1 = Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR Bit-1:
0 = No change.
1= Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR Bit-2:
0= No change.
1 = Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR Bit-3:
0= No change.
1= Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When the 16650 is in 16450 mode (FCR bit 0 = 0) or in the FIFO mode (FCR bit 0 = 1, FCR bit 3 = 0)when there are no characters in the transmit FIFO or transmit holding register the TXRDY* pin will go low. Once active, the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When the 16650 is in 16450 mode (FCR bit-0 = 0) or in the FIFO mode (FCR bit - 0 = 1, FCR bit-3 = 0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active, the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When the 16650 is in FIFO mode (FCR bit-0 = 1, FCR bit-3 = 1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When the 16650 in in FIFO mode (FCR bit-0 = 1, FCR bit-3 = 1) and the trigger level or the time-out has been reached, the RXRDY* pin will go low. Once it is activated, it will go high (inactive) when there are no more characters in the FIFO.

FCR Bit 4-5:
These bits are used to set the trigger level for the transmit FIFO interrupt. The 16650 will issue a transmit empty interrupt when the number of characters in the FIFO drops below the selected trigger level.

Bit - 5	Bit - 4	FIFO trigger level
0	0	16
0	1	8
1	0	24
1	1	30

FCR bit 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

Bit - 7	Bit - 6	FIFO trigger level
0	0	8
0	1	16
1	0	24
1	1	28

LINE CONTROL REGISTER (LCR)

The line control register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR Bit 1-0:
These two bits specify the word length to be transmitted or received.

Bit - 1	Bit - 0	Word Length
0	0	5
0	1	6
1	0	7
1	1	8

LCR Bit-2:
The number of stop bits can be specified by this bit.

Bit-2	Word Length	Stop Bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR Bit - 3:
Parity or no parity can be selected via this bit.
0 = no parity.
1= a parity bit is generated during the transmission, receiver also checks for received parity.

LCR Bit -4:
If the parity bit is enabled, LCR Bit-4 selects the even or odd parity format.
0 = ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1 = EVEN parity bit is generated by forcing an even number of 1's in the transmitted data, receiver also checks for same format.

LCR Bit 5:
If the parity bit is enabled, LCR bit-5 selects the forced parity format.
LCR Bit-5 = 1 and LCR Bit-4 = 0 , parity bit is forced to "1" in the transmitted and received data.
LCR Bit-5 = 1 and LCR Bit -4 = 1, parity bit is forced to "0" in the transmitted and received data.

LCR Bit-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to a low state).
0 = normal operating condition.
1= forces the transmitter output (TX) to go low to alert the communication terminal.

LCR Bit -7:
The internal baud rate counter latch and enhanced feature mode enable (DLAB).
0 = Normal operation.
1 = Divisor latch and enhanced feature register enable.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR Bit -0:
0 = force DTR* output to high.
1 = force DTR* output to low.

MCR Bit -1:
0 = force RTS* output to high.
1 = force RTS* output to low.
RTS* is used as a hardware flow control signal when enabled via EFR bit-6. RTS* goes high when FIFO has reached the selected trigger level and goes low as soon as the content of the receive holding register is below the trigger level. Content of this register changes with the state of the hardware flow control. It functions normally when hardware flow control is disabled.

MCR Bit -2:
0 = set OP1* output to high.
1 = set OP1* output to low.

MCR bit - 3:
0 = set OP2* output to high (STD mode). Forces INTx outputs to three state mode during PC mode selection.
1 = set OP2* output to low (STD mode). Sets the INTx outputs to active mode during PC mode selection.

MCR Bit-4:
0 = normal operating mode.
1 = enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode, the

register. Note that the character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR Bit - 2:
0 = no parity error (normal).
1 = parity error, received data does not have correct parity information. In the FIFO mode, this error is associated with the character at the top of the FIFO.

LSR Bit - 3:
0 = no framing error (normal).
1 = framing error received, received data did not have a valid stop bit. In the FIFO mode, this error is associated with the character at the top of the FIFO.

LSR Bit-4:
0 = no break condition (normal).
1 = receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR Bit-5:
It indicates that the 16650 is ready to accept a new character for transmission. In addition, it causes the 16650 to issue an interrupt to the CPU when the transmit holding register empty interrupt enable is set.

0 = transmit holding register is not empty.
1= transmit holding register (or FIFO) is empty. CPU can load the next characters. When this bit is set, CPU can load up to 32 bytes of data to the 16650.

LSR Bit-6:
0 = transmitter holding and shift registers are full.
1 = transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR Bit - 7:
0 = normal.
1 = at least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR Bit - 0:
Indicates that the CTS* input to the 16650 has changed state since the last time that it was read.

MSR Bit -1:
Indicates that the DSR* input to the 16650 has changed state since the last time that it was read.

MSR Bit-2:
Indicates that the RI* input to the 16650 has changed from a low to a high state.

MSR Bit-3:
Indicates that the CD* input to the 16650 has changed state since the last time that it was read.

MSR Bit-4:
This bit is equivalent to RTS in the MCR during local loop back mode. It is the compliment of the CTS* input.
CTS* functions as a hardware flow control signal input if it is enabled via EFR bit-7. Transmit holding register is gated with this input to start/stop the transmission. A high at this pin will stop the transmission as soon as a complete character is transmitted.

MSR BIT - 5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR Bit - 6:
This bit is equivalent to OP1in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR Bit-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment of the CD* input.

Note: Whenever MSR Bit 3-0: is set to logic "1", a modem status interrupt is generated.

Scratchpad Register (SR).

The 166509 provides a temporary data register to store 8 bits of information for variable use.

Enhanced feature register (EFR).

Enhanced features can be enabled/disabled via this register.

EFR Bit 0 - 3:
Combinations of software flow control can be selected by programming these bits.

Co

0

1

0

1

X

X

X

0

1

0

Cont-3	Cont-2	Cont-1	Cont-0	Tx, Rx software flow controls
0	0	X	X	No transmit flow control.
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1 and Xon2: Xoff1, Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1
X	X	0	1	Transmit Xon1, Xoff1. Receiver compares Xon1 or Xon2
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmits Xon1 and Xon2 : Xoff1 and Xoff2 Receiver compares Xon1 and Xon2: Xoff1 and Xoff2.
0	0	1	1	No transmit flow control. Receiver compares Xon1 and Xon2: Xoff1 and Xoff2.

EFR Bit-4:
Enhanced interrupt control bit.
0 = disables the IER bits 4-7 and ISR bits 4-5. Standard 16550 mode.
1 = Enables the enhanced interrupt functions.

EFR Bit-5:
0 = Normal.
1 = Special character detect. 16650 compares the incoming receive data with Xoff-2 data. Up on correct match, the received data will be transferred to FIFO and ISR Bit-4 will be set to indicate detection of special character.

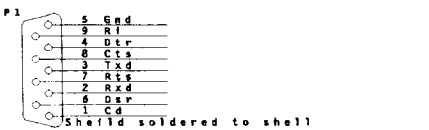
EFR Bit -6:
RTS* flow control.
0 = Normal. RTS* flow control is disabled. Standard 16550 mode.
1 = RTS pin goes high when the number of characters in the receive FIFO reach the programmed trigger level.

EFR Bit-7:
CTS* flow control.
0 = Normal. CTS* flow control mode is disabled. Standard 16550 mode.
1 = transmission is resumed when low input signal is detected on the CTS* pin.

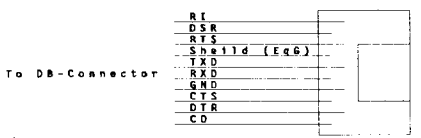
REGISTERS	RESET STATE
IER	IER BITS 0-7 = 0
ISR	ISR BIT-0 = 1, ISR Bits 1-7 = 0
LCR	LCR Bits 0 - 7 = 0
MCR	MCR Bits 0 - 7 = 0
LSR	LSR BITS 0 -4 = 0 LSR BITS 5-6 = 1 LSR Bit 7 = 0
MSR	MSR Bits 0 - 3 = 0, MSR Bits 4 - 7 = input signals
FCR	FCR Bits 0 - 7 = 0
FER	FER Bits 0 - 7 = 0

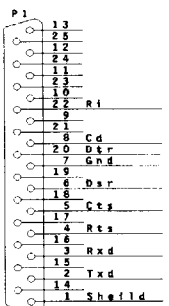
A2,A1,A0	Register	Bit–7	Bit–6	Bit–5	Bit–4	Bit–3	Bit–2	Bit–1	Bit–0
0 0 0	RHR	bit–7	bit–6	Bit–5	Bit–4	Bit–3	Bit–2	Bit–1	Bit–0
0 0 0	THR	bit–7	bit–6	Bit–5	Bit–4	Bit–3	Bit–2	Bit–1	Bit–0
0 0 1	IER	0/CTS interrupt	0/RTS interrupt	0/XOFF interrupt	0/Sleep Mode	modem status interrupt	Receive line status interrupt	Transmit holding register empty interrupt	Receive holding register interrupt
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0/TX trigger (MSB)	0/TX trigger (LSB)	DMA mode select	XMIT FIFO reset	Receive FIFO reset	FIFO enable
0 1 0	ISR	0/FIFOs enabled	0/FIFOs enabled	0/RTS,CTS	0/XOFF	INT priority bit 2	INT priority bit 1	INT priority bit 0	INT status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit–1	Word length bit–0
1 0 0	MCR	Clock Select	0	INT A type select	loop back	OPT2*/IRQx enable	OP1	RTS	DTR
1 0 1	LSR	0/FIFO error	transmitter shift register empty	transmitter holding register empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD	delta RI	delta DSR	delta CTS
1 1 1	SPR	bit–7	bit–6	Bit–5	Bit–4	Bit–3	Bit–2	Bit–1	Bit–0
0 0 0	DLL	bit–7	bit–6	Bit–5	Bit–4	Bit–3	Bit–2	Bit–1	Bit–0
0 0 1	DLM	bit–15	bit–14	Bit–13	Bit–12	Bit–11	Bit–10	Bit–9	Bit–8
0 1 0	EFR	AUTO CTS	AUTO RTS	Special Character select	Enable IER bits 4–7, ISR, FCR bits 4–5, MCR bits 5,7	cont–3 TX, RX control	cont–2 TX, RX control	cont–1, TX, RX control	cont–0, TX, RX, control

Gtek Card



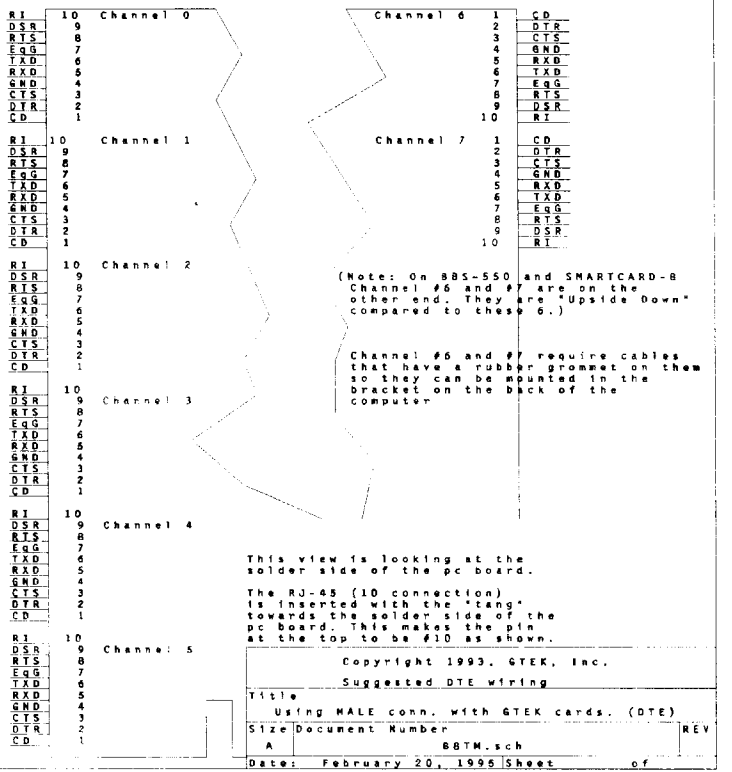
DB9 Male
Like a Computer Connection
to a modem





DB-25 MALE
Like a Computer Connection
To A Modem

Warning: Don't expect the WIRE COLORS to always be the same from one cable to another!



(Note: On BBS-550 and SMARTCARD-8 Channel #6 and #7 are on the other end. They are "Upside Down" compared to these 6.)

Channel #6 and #7 require cables that have a rubber grommet on them so they can be mounted in the bracket on the back of the computer

This view is looking at the solder side of the pc board.

The RJ-45 (10 connection) is inserted with the "tang" towards the solder side of the pc board. This makes the pin at the top to be #10 as shown.

Suggested DTE wiring

Title
Using MALE conn. with GTEK cards. (DTE)

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